Design of Low Power CMOS VCO Having Low Phase Noise

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Abstract— The growing demand for high-speed wireless connectivity has accelerated the development of data-centric third-generation (3G) services, particularly the wireless local area network (WLAN) communications protocols such as the Institute of Electrical and Electronics Engineers (IEEE) standard 802.11a and the European Telecommunications Standardization Institute (ETSI) standard HiperLAN2. To support the increasingly faster data rates and to combat the less favorable propagation conditions at higher carrier frequencies, these standards employ the more complex modulation scheme of orthogonal frequency division multiplexing (OFDM). With OFDM, the carrier is subdivided into several individually modulated orthogonal subcarriers, all of which are simultaneously transmitted [1]-[4]. However, a higher data rate is often accompanied by more sensitivity to phase errors for a particular modulation scheme. This increased sensitivity is inevitably translated into more stringent phase noise requirements for the voltage-controlled oscillator (VCO). The VCO is an integral and critical part of the transceivers of modern communications systems.

I. INTRODUCTION

In CMOS technologies, a fully-integrated VCO can be implemented as a ring oscillator, an active inductor-capacitor (LC) oscillator, or a passive LC oscillator. A VCO using a transmission-line resonator can also be realized for better phase-noise performance, but it is generally not considered because of the large-area requirement. The ring oscillators are typically implemented with an odd number of inverter stages connected in series, forming a positive feedback configuration. They are attractive because of their ease of implementation and large tuning range. However, they suffer from poor phase-noise performance and are generally not suitable for communications applications. The active LC oscillators employ LC resonators as the frequency-determining elements, where the inductors are implemented with capacitance and active devices in a gyrator-C circuit topology. The active inductors are capable of very large quality factors (Q).

But the noise contribution from the active devices, causes the phase noise of the oscillator to be relatively high, compared to its passive counterpart, and is therefore not suitable for low-noise design applications. Similarly, the passive LC oscillators employ passive LC resonators as their frequency-determining elements. Of this type of circuit, the complementary cross-coupled transconductor LC VCO of is arguably the most ubiquitous circuit topology because it can be implemented entirely on-chip and it provides reasonably good phase-noise performance. It is also attractive for low-power design resulting from sharing the bias current between the NMOS and PMOS transconductors. Its drawback is the relatively low output voltage swing because of the voltage drop across the bias current transistor M5. To alleviate this problem, it is possible to eliminate either the NMOS or the PMOS transconductor. The output signal swing is increased, and the noise contribution from the active devices is lower (the number of transistors is halved). However, for the same bias current and operation in the current-limited regime, the output swing of the NMOS-only (PMOS-only) topology is theoretically only half that of the complementary circuit. As a result, the phase-noise performance of the latter is generally more superior.

II. SCOPE OF RESEARCH

As demonstrated in the previous section, the phase noise of a CMOS LC VCO can be greatly improved by reducing the flicker noise of its bias transistor. Therefore, it is reasonable to expect that further improvement can be achieved by canceling out all flicker noise sources present in the VCO circuit, which will be the objective of this thesis. This noise cancellation technique is based on the linear time-variant phase noise model presented by Hajimiri and Lee. For each noise source in the circuit, there is a corresponding periodic impulse sensitivity function (ISF) describing the conversion mechanism of this circuit noise into phase noise. The VCO output excess phase caused by this source can be calculated by convolving its noise function with the ISF.
The VCO close-in phase noise is then proportional to the product of the DC component of the ISF and the integral of the low-frequency portion of the noise function. Therefore, if the circuit can be designed such that the ISF corresponding to each transistor noise source has no DC component, the flicker noise will not have any effect on the phase noise of the VCO. In order to achieve good noise cancellation result, an iterative design approach, requiring accurate phase-noise simulation methodology, is necessary. The simulation method involves a transient analysis to obtain the ISF of a noise source, several additional miscellaneous analyses to characterize this noise source and its cyclostationary properties if necessary, and a post-processing algorithm combining all simulated results to calculate the VCO phase noise excited by this noise source. Finally yet importantly, the resulting circuit topology provides an additional benefit for quadrature VCO design. It allows capacitive coupling of the individual VCOs, thereby avoids any phase-noise degradation that exists in the typical parallel- or series-quadrature VCO topologies.

III. NEW LOW-PHASE-NOISE CMOS LC VCO

Circuit topology can greatly affect the phase noise performance of an oscillator. In this chapter, a new low-phase-noise CMOS LC VCO is presented. Unlike some of the other approaches that attempt to reduce phase noise by attenuating the flicker noise sources, this new topology seeks to cancel the effect of low-frequency noise altogether by tuning the appropriate circuit parameters such that the ISF corresponding to a particular noise source does not contain any DC component. Therefore, the upconversion of flicker noise into phase noise is inhibited.

The new circuit also reduces the strength of the noise sources by operating the switching transistors in the active/subthreshold region, where the noise spectral density is less than that of the devices operating in the saturation region. Additionally, the effect of thermal noise on the phase noise is minimized, i.e. the magnitude of the ISF waveform is minimized by concentrating the energy of the noise source near the peak of the output signal where its phase is least sensitive to noise perturbation. Lastly, the new circuit topology allows quadrature implementation of the VCO via capacitive coupling. Therefore, little or no phase noise degradation occurs since there are no additional active devices.

**Circuit Analysis**

Figure 3.1 shows a simplified schematic of the new VCO circuit. As can be seen, this is a variation of the cross-coupled transconductance VCO, where the bias transistor has been eliminated. MOS capacitors are inserted in the cross-coupled connecting paths, so that they form capacitive divider networks with the equivalent input capacitance of the switching transistors (gate-source capacitance plus Miller capacitance). The divider networks attenuate the driving signals of the switching transistors, thereby allowing their aspect ratios to be increased substantially without forcing the oscillator into the voltage-limited regime, the undesirable mode of operation where power is wasted because of output voltage clipping. The large W/L ratio keeps the transistors operating in the triode region even when conducting significant amount of current. This is quite beneficial because in this region, the transistor generates much less flicker noise than it does in the saturation region. This point is illustrated in Figure 3.2, which depicts the simulated noise spectral density for two NMOS transistors in the National Semiconductor Corp. (NSC) CMOS9 process with minimum length (180 nm) and width of 48 μm and 450 μm respectively, each carrying a drain current of 2 mA. Flicker noise in CMOS transistors is generated by the trapping and detrapping of carriers in the oxide layer. When a transistor operates in the triode/subthreshold region, a weak inversion channel is established under the oxide layer where the carrier concentration is substantially less than that in the strong inversion channel formed when the transistor is saturated. Additionally, the vertical electric field over the gate is smaller for the triode/subthreshold region than for the saturation region because of the smaller \( V_{GS} \).
These two factors combine to reduce the probability of carrier trapping events, thus reducing the flicker noise of the device.

Figure 3.1 Simplified schematic of the new low-phase-noise VCO

Figure 3.2 Noise spectral density of two NMOS transistor with the same drain current (2 mA), one in the saturation region, the other in the triode region

These inserted MOS capacitors (feedback capacitors) eliminate the DC feedback paths from the output nodes of the VCO to the gates of the transconductors. Therefore, the resistor network R1-R3 is needed to bias the transconductors. To minimize the effect of circuit noise on the phase noise, the transconductors can be biased below the threshold voltages of the transistors so that the conducting drain current is relatively small near the zero-crossing points of the output waveform, where it is most sensitive to noise perturbation. However, in practice, the propagation delay (from $v_{gs}$ to $i_d$) of the transistor shifts the current waveform (Figure 5.3) such that the drain current at one of the zero-crossing point is significantly increased (at phase angle=$\pi$), thereby diminishing this benefit.

Nevertheless, this biasing scheme still provides on average lower drain current near the zero-crossing points than that of the cross-coupled transconductance VCO with fixed bias transistor. Additionally, because of the larger W/L ratio, the corresponding noise spectral density is lower for the same drain current, further reducing the phase noise.

IV. PHASE NOISE ANALYSIS

Figure 4.1 depicts the new VCO circuit with all the noise sources. The noise generated by the isolation inductors (L1-L4) is ignored since it is negligible compared to that generated by the bias resistors. On the other hand, the noise contribution of the parasitic series resistance of the resonator is similar to that described in the previous chapter, i.e., for low-Q system (<10) and low-phase-noise circuit topology, it must be taken into account. In fact, for the new VCO circuit proposed in this work and an inductor with a quality factor of about eight at 5.5 GHz, this noise source may be the most dominant, even at close-in offset frequency. Therefore, it is critical to have an optimal layout for the on-chip inductor and on-chip varactor as well as for the trace wiring between these two components.

Figure 4.1 Schematic of new VCO with noise sources.

Similarly, the thermal noise sources of the bias resistors (R1-R3) must also be considered carefully. In this case, it is a tradeoff between power dissipation and noise contribution. As mentioned previously, these noise sources are amplified and injected into the resonator by the NMOS and PMOS transistors but with opposite polarity.
Thus, there is some partial cancellation of the noise signals at the terminals of the resonator. Therefore, the effect they have on the phase noise is reduced. Because of this, relatively low bias current (less than one milliamp) is possible without any degradation of the phase noise generated by the active devices. Compared to the conventional VCO design, the current mirror adds 3 dB to the phase noise generated by the bias transistor for unity-current gain. To have negligible phase noise degradation, the current gain has to be less than one half. It means that the current in the mirror transistor has to be at least twice that of the bias transistor, a significant penalty in power dissipation.

The phase noise contribution of transistors M1 and M3 is analyzed next. Similar analysis can be applied for transistors M2 and M4 by symmetry. To cancel out the effect of flicker noise, the ISF corresponding to the noise source of M1 and M3 must not have any DC component. This can be accomplished with proper sizing of the NMOS and PMOS transistors as well as the cross-coupled feedback capacitors.

V. Design Procedure

A recursive approach to designing the new VCO without the flicker-noise effect is necessary because it is difficult to derive analytically the ISF of the noise sources and the propagation delays of the switching transistors, the two most important elements for the optimization of phase noise performance.
A new VCO circuit topology that allows the cancellation of low-frequency flicker noise effect on the VCO phase noise. The proposed circuit will allow the designer to select the transistor sizes, the feedback ratios, and the bias voltages such that the effective ISF corresponding to the transistors’ noise source has no DC component, thus preventing the up conversion of flicker noise into phase noise.

A step-by-step design algorithm will be presented to help the designer to achieve optimal design in a simple straightforward fashion.

A simulation methodology will be presented that helps in the previously mentioned design algorithm. A MATLAB script is included to help in the computation of the ISF and the oscillator phase noise.

REFERENCES


