Grid Connected PV By Using Transformerless Inverter With Implicit DC Bus

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Abstract— To remove a common-mode leakage current in the transformer less photovoltaic (PV) system, virtual DC bus concept is used in this paper. Here grid neutral line is directly connected to the negative pole of the dc bus. The stray capacitance present in the PV panels is grounded. Through this concept ground leakage current can be suppressed completely. The virtual dc bus is created to provide negative ac grid current. Here the dc bus voltage is still the same as that of the full-bridge inverter. The virtual dc bus is realized with the switched capacitor technology. It consists of five switches, two capacitors, and a single filter inductor. The gate pulses are generated using uni-polar sinusoidal pulse width modulation (SPWM) and the double frequency SPWM techniques.

Keywords— Common mode (CM) current, Photovoltaic (PV) system, Switched capacitor, Transformerless inverter, Unipolar sinusoidal pulse width modulation (SPWM), Virtual dc bus.

I. INTRODUCTION

The distributed photovoltaic (PV) power generation systems have most popularity in both the commercial and residential areas. In many cases, the inverters are used to feed the PV power into the utility grid.

Due to high price of the PV panels. Small size is used for the low-power and single-phase systems. In the traditional grid-connected PV inverters, either a line frequency or very high-frequency transformer is used to provide a good isolation between the grid and the PV panels. Eliminating an isolation transformer can be a best solution for increasing the efficiency and decrease the size and cost. If the transformer is removed, the common-mode (CM) ground leakage current will appear on the parasitic capacitor between the PV panels and the ground. The CM current may decrease an efficiency of power conversion, also raise the grid current distortion, and degrade an electric magnetic compatibility. The CM current path direction in the grid-connected transformer-less PV inverter system is shown in Fig.1. It is created by power switches, filters, ground impedance, and the parasitic capacitance coupled between PV panels and ground. The CM voltage VCM is defined by

$$v_{CM} = \frac{v_{AO} + v_{BO}}{2} + \frac{(v_{AO} - v_{BO}) (L_2 - L_1)}{2(L_1 + L_2)}$$  (1)

Where VAO is the voltage difference between A and O, VBO is the voltage difference between B and O, and L1 and L2 are the output filter inductors.
II. DERIVED TOPOLOGY AND MODULATION STRATEGY

Based on the virtual dc bus concept, a novel inverter topology is used in proposed methodology. It consists of five power switches $S_1$ to $S_5$ and one single filter inductor $L_f$. The PV panels and capacitor $C_1$ form a real dc bus while the virtual dc bus is provided by $C_2$. Capator $C_2$ is charged by dc bus through switches $S_1$ and $S_3$ to maintain a constant voltage. This topology can be simulated with the unipolar SPWM and double-frequency SPWM.

A. Uni-polar SPWM

The waveform for the unipolar SPWM of the proposed inverter is shown in Fig.3. The gate signals for the power switches are generated by comparing the modulation wave and the carrier wave. During positive half cycle, modulated wave is greater than zero. Switches $S_1$ and $S_3$ are turned ON and switch $S_2$ is turned OFF. Capacitors $C_1$ and $C_2$ are parallel connected. During negative half cycle, modulated wave is lesser than zero. Switch $S_5$ is turned ON and switch $S_4$ is turned OFF. $S_1$ and $S_3$ turned OFF with the carrier frequency synchronously. The negative voltage is generated by the virtual dc bus $C_2$ and the inverter output is at negative voltage level. At state 2, switches $S_1$ and $S_3$ are turned ON while switch $S_2$ is turned OFF. The inverter output voltage $V_{AN}$ equal to zero; meanwhile, $C_2$ is charged by dc bus using switches $S_1$ and $S_3$.

B. Double-Frequency Sinusoidal PWM

The proposed topology can also work with double-frequency Sinusoidal PWM to achieve a higher switching frequency, as shown in fig.4. In the double-frequency SPWM, the five power switches are divided into two parts, and they are modulated with two inverse sinusoidal waves respectively. Switches $S_1$, $S_2$ and $S_3$ are compared with $u_{g1}$, while $S_4$ and $S_5$ are compared with $u_{g2}$.

For all of the four operation states, there is no limitation on the direction of the output current $i_{grid}$, since the power switches with anti parallel diodes can produce bidirectional current flow. The proposed topologies have the capability of feeding reactive power into the grid to help support the stability of the power system.
In the traditional grid-connected PV inverters, either high-frequency or a line frequency transformer is used for providing isolation between the grid and the PV panels. For a typical PV array, the output voltage is very low, and a high voltage gain is used for grid-connected function.

### III. SIMULATION RESULTS

In Fig.6 the gate pulses are generated using uni-polar sinusoidal pulse width modulation technique. The output voltage and output current waveforms are shown in Fig.7.

<table>
<thead>
<tr>
<th>TABLE I</th>
<th>POWER DESIGN PARAMETERS</th>
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<tbody>
<tr>
<td>Full PV output power</td>
<td>300 W</td>
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<tr>
<td>Input voltage</td>
<td>20-40 V</td>
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<tr>
<td>Output voltage</td>
<td>400 V</td>
</tr>
<tr>
<td>Switch frequency</td>
<td>50 KHz</td>
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</tbody>
</table>
In Fig. 8 the gate pulses are generated using double frequency sinusoidal pulse width modulation technique. The output voltage at grid and output current waveforms are shown in Fig. 9.

In Fig. 10 the gate pulses are generated using PI controller. The output voltage at grid and output current waveforms is shown in Fig. 11.
method is suitable for low-power single-phase applications, where the output current is low. For eliminating the CM current, the virtual dc bus concept gave a best solution for the transformer less grid-connected PV inverters.

References


