Design of Two-Stage CMOS Operational Amplifier

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Abstract—This paper presents a design of Two Stage CMOS operational amplifier, which operates at ±2.5V power supply using umc 2µm CMOS technology. The OP-AMP designed is a two-stage CMOS OP-AMP. The OP-AMP is designed to exhibit a unity gain frequency of 4.416MHz and exhibits a gain of 96dB with a 700 phase margin. Design and Simulation has been carried out in LT Spice tools.

Keywords—2 stage CMOS op-amp, design, simulation and results.

I. INTRODUCTION

The designing of high performance analog integrated circuits is becoming most essential with the continuous trend towards the reduced supply voltages and transistor channel length. MOS is most success among all because it can be scaled down to smaller dimensions for higher performance. The size can be reduced to micrometer or nanometer for getting higher performance. On scaling down the Transistor size the most important advantage is we can integrate more number of transistor on the same size and we can get a faster amplifier compared to previous one. This leads to continuous growth of the processing capacity per chip and operating frequency.

In most of the electronics circuits the Operational Amplifiers is the most common building blocks. So as the transistor channel length and power supply is reduced then the design of Op amps face continuous challenge. Due to different aspect ratio(W/L), there is a tradeoff among speed, gain, power and the other parameters. The implementation of a CMOS OPAMPs that combines a considerable dc gain with higher unity gain frequency has been a most difficult problem. There have been several circuits proposed to evaluate this problem. The purpose of the design methodology in this paper is to propose accurate equations for the design of high-gain 2 staged CMOS op-amp.

For this, a simple analysis with some meaningful parameters (such as gain bandwidth, phase margin, etc.) is performed. The method handles wide variety of specifications and constraints. In this, we formulate the CMOS op-amp design problem and their aspect ratios. The method we present can be applied to a wide variety of amplifier structures, but in this paper we apply the method to a specific two stage CMOS op-amp. The variation in the performance of the op-amp with variations in the width and length of the CMOS and the effect of scaling the gate oxide thickness is discussed. The simulation results have been obtained by umc 2µm CMOS technology. High gain in operational amplifiers is not the only desired figure of merit for all kind of signal processing applications.

In this case, the slew rate will increase for an increase in current. Thus, we can conclude that the selection of device sizes depends on trade-offs between stability and slew-rate.

II. BLOCK DIAGRAM OF TWO STAGE CMOS OP-AMP

Operational Amplifiers are the backbone for many analog circuit designs. The speed and accuracy of these circuits depends on the bandwidth and DC gain of the Op-amp.

![Fig(1). Block diagram two stage CMOS Op Amp](image-url)
Larger will be the bandwidth and gain, higher will the speed and accuracy of the amplifier. The general block diagram of an op-amp with an output buffer is shown above in Figure(1).

![Block Diagram](image)

**Figure(2): Simplified Block Diagram**

The simplified Block Diagram is shown in figure(2). The first block is a differential amplifier. It has two inputs, that are the inverting and non-inverting voltage. It gives a differential voltage at the output or a differential current which depends only on differential input voltage. The next block is a differential ended to single-ended converter. It is used to transform the differential signal generated by the first block into a single ended output signal. Some architecture doesn’t require the differential to single ended function; therefore this block can be eliminated in that.

In circuits where, the gain provided by the input stages is not sufficient, so there is an additional amplification is required which is provided by the second stage, i.e. the common source amplifier, driven by the first stage output. As this stage uses differential input unbalanced output differential amplifier, so it provides the required extra gain. The biasing circuit is here to provide the proper operating point to each transistor in its saturation region. The output buffer stage provides the low impedance at output and larger output current needed to drive the load of op-amp or improves the slew rate. Even the output stage can be dropped since many applications do not need low output impedance. If the op-amp is intended to drive a small purely capacitive load, then output buffer is not required. When the output stage is not used the circuit is an operational transconductance amplifier, OTA. The motive of the compensation circuit is to decrease the gain at high frequencies and to maintain stability when negative feedback is applied to the op amp.

**A. Circuit Operation**

The final circuit designed to satisfy the specifications is shown in Figure(3).

![Circuit Diagram](image)

**Figure(3): The circuit chosen for this Op-Amp design**

**B. Differential Gain Stage**

Transistors M1, M2, M3, and M4 constitute the first stage of the op amp the differential amplifier. The gate of M1 is the non-inverting input and of M2 is the inverting input. A differential input signal is applied across the two input terminals will be amplified according to the gain of the differential stage. The gain of this stage is the transconductance of M1 times the total output resistance seen at the drain of M2. The main resistances that contribute to the output resistance are that of the input transistors themselves and also the output resistance of the load transistors, M4 and M3. The current mirror active load used in this circuit has three main advantages. First, the use of active load devices creates a large output resistance in a relatively small amount of chip area. The current mirror topology performs the differential to single-ended conversion of the input signal, and finally, the load helps with common mode rejection ratio. In this, the conversion from differential to single ended is achieved by using a current mirror (M4 and M3). The current from M1 is mirrored by M3 and M4 and subtracted from the current from M2. Finally, the differential current from M1 and M2 multiplied by the output resistance of the input stage gives the single-ended output voltage, which is the part of the input to the next stage.
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C. Common Source Second Gain Stage

The second stage is a current sink load inverter. The motive of the second gain stage is to provide additional gain consisting of transistors M6 and M7. This stage receives the output from the drain of M2 and amplifies it through M6 by common source configuration. This stage employs an active device, M7, which serve as the load resistance for M6. The gain of this stage is the transconductance of M6 times the equivalent load resistance seen at the output of M6 and M7. M6 is the driver while M7 acts as load.

D. Biasing Circuit

Transistors M8 and a reference current source form a simple current mirror biasing network that provides a voltage between the gate and source of M5 and M7. Transistors M5 and M7 sink a current based on their gate to source voltage which is controlled by the bias network.

III. DESIGN OF THE 2 STAGE OP-AMP

The first aspect considered in the design was to meet the desired specifications. Based on a clear understanding of the specifications, we have chosen the standard CMOS op-amp circuit topology in our design.

<table>
<thead>
<tr>
<th>Specification Names</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply VDD</td>
<td>± 2.5V</td>
</tr>
<tr>
<td>Gain</td>
<td>≥ 60dB</td>
</tr>
<tr>
<td>Gain Bandwidth</td>
<td>4MHz</td>
</tr>
<tr>
<td>Settling Time</td>
<td>1u Sec</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>10V/uSec</td>
</tr>
<tr>
<td>Input common Mode</td>
<td>(-1V)–2V</td>
</tr>
<tr>
<td>Common mode rejection</td>
<td>≥60dB</td>
</tr>
<tr>
<td>Output Swing</td>
<td>1 – 2.4V</td>
</tr>
<tr>
<td>Offset</td>
<td>≤10m</td>
</tr>
</tbody>
</table>

A. Design Methodology Of Op-Amp

Formula used:

Slew Rate = \( \frac{I_s}{C_c} \)

First stage gain (A\text{v1}) = \( \frac{g_{m1}}{g_{ds2} + g_{ds4}} = \frac{2g_{m1}}{I_s(\lambda_2 + \lambda_4)} \)

Second stage gain (A\text{v2}) = \( \frac{g_{m6}}{g_{ds6} + g_{ds7}} = \frac{2g_{m6}}{I_6(\lambda_6 + \lambda_7)} \)

Gain Bandwidth product = \( \frac{g_{m1}}{C_c} \)

Output pole p\text{2} = \( \frac{g_{m6}}{C_c} \)

RHP zero \( z_1 = \frac{g_{m6}}{C_c} \)

60° phase Margin requires that \( g_{m6} = 2.2g_{m2} \) (CL/Cc) if all the roots are ≥10GB

Positive ICMR:

\( V_{in(max)} = V_{DD} - \sqrt{\frac{I_s}{\beta_1}} - |V_{Tos}|_{max} + V_{T1(min)} \)

Negative ICMR:

\( V_{in(min)} = V_{SS} + \sqrt{\frac{I_s}{\beta_1}} + |V_{Tos}|_{max} + V_{DS(sat)} \)

\( g_{m1} = g_{m2} = g_{m3}, g_{m6} = g_{m7} \)

\( g_{ds2} + g_{ds4} = GI, \) and \( g_{ds6} + g_{ds7} = GH \)

The assumptions we have taken that all transistors are in saturation. In this project a two-stage op amp with n-channel input pair is designed. The op amp uses a dual polarity power supply (VDD and VSS) for ac signals can swing above and below ground and also be centered at ground.

The calculation results provided the estimated parameters (such as transistor width and length, capacitance, etc.) to make the circuit schematic (shown in figure 4) in LT Spice.
IV. SIMULATION RESULTS

A. Transient Analysis

Here \( C_c = 12 \text{pF} \) and \( C_l = 10 \text{pF} \).

The input applied to differential Amplifier is a 1mV and we are getting an output of 2.4 V. The simulated output is shown in Figure (5).

B. AC Analysis

In AC analysis we examine the Gain, Phase Margin and Gain band width product.

- Start frequency = 1Hz
- Stop frequency = 100 KHz

Gain= 96dB, \( \omega_{-3dB} = 70 \text{Hz} \)
Phase Margin= 70°
Reference circuit have \( L=2\text{um} \).

This op-amp have a maximum noise level at output is \( 1.5\text{mV/Hz}^{1/2} \), which is a very small and the graph clearly shows that the noise level at output decreases as the frequency is increases.

Figure (4). Schematic design of 2-stage CMOS Op-Amp

Figure (5). Simulated output of op-amp

Figure (6). Frequency Response curve of op-amp

Figure (7). Noise Simulated at output of op-amp
<table>
<thead>
<tr>
<th>W/L Ratio</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>W1, W2</td>
<td>6</td>
</tr>
<tr>
<td>W3, W4</td>
<td>40</td>
</tr>
<tr>
<td>W5, W8</td>
<td>32</td>
</tr>
<tr>
<td>W9</td>
<td>10</td>
</tr>
<tr>
<td>W7</td>
<td>70</td>
</tr>
<tr>
<td>W6</td>
<td>360</td>
</tr>
</tbody>
</table>

V. CONCLUSION

This paper presented the full design and analysis of a two stage CMOS Op-Amp. The results shows that the amplifier designed has successfully satisfied all the design specification given in advance.

REFERENCES