A Low Power Low Noise Two Stage CMOS Operational Amplifier for Biopotential Signal Acquisition System

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Abstract—Monitoring of the biopotential signals in present scenario attract much attention to the researcher due to increasing demand for better quality of life and to enhance interaction between humans and machines. Biopotential signals are relatively weak amplitude and low frequency in nature. Therefore it is required to design a front circuitry that defines quality of signal for processing to the next block (ADC). This paper presents a design procedure by using the Equivalent Circuit Approach (ECA) for a low power, low noise, and rail-to-rail output swing Operational Amplifier (Opamp) which is used at the front end circuitry of Biopotential signal acquisition systems. A differential pMOS input stage is used for noise cancellation and a common source stage is used at the output for high output swing. The opamp is experimentally validated through TSMC 90nm CMOS process Technology and a comparison is carried out with previous designs. This opamp exhibits input referred noise of 28nV/√Hz, Phase Margin =83°, B.W=10.1 kHz and power consumption 91µW for 40µA external bias current. Importantly, all these advantages are achieved at the cost of little Gain deviation.

Keywords—Biopotential Signal, Equivalent Circuit Approach (ECA), Low noise, Low power, Opamp, Rail-to-rail

I. INTRODUCTION

As CMOS Technology shrinks towards Nanoscale regime, there is an increasing demand for more advanced and effective medical devices due to the interest on real-time personal home health monitoring [1],[2]. These devices usually contain various types of biosensors, CMOS operational amplifier is one of important block at the front-end of these biosensors [2], [3]. Because most bio-potential signals are characterized by their relative weak amplitude and low frequency, usually of few mV or less and the frequency in the range of less than 1 kHz [2],[4]. Biopotential signals are distorted due to Noise produced at the interface between skin and electrode of the Biosensor [5]. So, before forwarding these biosignals, further amplification and filtering is needed to minimize noise and amplify bio-potential signals only [2], [7].

To maintained proper SNR throughout the signal processing systems a operational amplifier with low noise, high output swing and high gain needs to be used [8]. Also there is need of amplifier which is compatible with standard CMOS technology to make the system fully integratable and low cost.

Figure 1. Biopotential Electronics Detecting System Block [4]

Our design approach is based on the technique proposed in [6], where a bulk biasing is used to achieve high gain and pseudo cascade compensation is used for stability enhancement. Moreover the circuit uses 1V supply voltage and 40µA external biasing current to increase the battery life-time efficiently.

This paper deals with the design procedure and the proposed CMOS equivalent circuit approach respectively and are depicted in Section II. Section III discusses the simulation results and comparison while Section IV describes the conclusion.

II. CIRCUIT DESIGN

The design presented in this paper has followed the principle of pseudo cascode as a compensation technique for stability enhancement and bulk biasing technique [6] to operate transistors in the weak inversion region which helps to achieve our design objectives.
The circuit schematic is shown in Fig.2.(a). This amplifier is composed of two stages. In the first stage pMOS differential input (M1, M2, M3, M4), the nMOS current mirror (M5, M6, M7, M8) and the pMOS supply stage (M9, M10), are used. In the second stage a common source stage consist of pMOS (M19, M20) and nMOS (M17, M18) are used for high output swing.

A equivalent circuit approach with details design procedure is given below in order to get our design motives. The main idea in our work is to dimension each one of these transistors in order to obtain the required performance for the amplification of bio signals, and to decrease the Flicker noise which dominates at low frequencies. Proper Sizing of transistors has taken care of because it is critical to achieve a low noise at a low current level with maintaining high gain. A proper biasing circuit with external 40µA current source is used to operate pMOS(M9,M19) and nMOS(M5,M6,M18) into sub threshold region for overall power consumption and high output swing.

A equivalent circuit configuration of Fig.2.(a) is shown in Fig. 2.(b) and then the design procedure is given below.

**In the equivalent circuit two assumptions are made throughout the design.**

**A. L=L₉+L₁₀ [6]**

Where L= equivalent transistor gate length and L₉, L₁₀ are Composite transistor gate length

**B. Cₑq ≥ C₁+C₂**

**Step 1:** Current through M5

\[ I_{MS} = SR \times C_{eq} \]

\[ V_{SD5} = V_{SG5} | V_{To} | = V_{DD} - V_{pb} - | V_{To} | \]

\[ \left( \frac{W}{L} \right)_{5} = \frac{2I_{SD5}}{K_{p}V_{SD5}^{2}} \]  

(1)

**Step 2:** From Gain bandwidth product

\[ \omega_{GB} = \frac{g_{m1}}{C_{eq}} = \sqrt{2K_{p}} \left( \frac{W}{L} \right)_{1,2} I_{SD1} \]

**Step 3:**

\[ \left( \frac{W}{L} \right)_{3,4} = \frac{2I_{DS3,4}}{K_{n}V_{G3,\text{min}}^{2} - V_{ss}^{2}} \]  

(3)

Where \( V_{G3,\text{min}} = V_{D1} = V_{S1} - V_{SD1} \)

Vₚᵣ is ground in Fig. 2.(b)

**Step 4:** Phase Margin

\[ PM = 90° - \tan^{-1} \frac{\omega_{GB}}{Z} - \tan^{-1} \frac{\omega_{GC}}{P_{2}} \]

Where

\[ \omega_{GC} = \frac{g_{m2}}{C_{eq}} \]

\[ Z = \frac{g_{m6}}{C_{eq}} \]

\[ P_{2} = \frac{g_{m6}}{C_{1} + C_{2}} \]

The condition is that Z > P₂ and Cₑq ≥ C₁+C₂.
To achieve Phase Margin >60° C_L > 2.2 C_eq must be satisfy and neglecting second pole.

\[ PM < 90° - \tan^{-1}\left(\frac{g_{m2}}{g_{m6}}\right) \]

\[ g_{m6} > \tan^{-1}\left(\frac{90° - PM}{2}\right) \]

\[ \left(\frac{W}{L}\right)_g = \frac{g_{m6}}{K_n V_{SD6}} \] (4)

Step 5: Current through transistor M6

\[ I_{DS6} = \left(\frac{W}{L}\right)_g I_{DS5} \]

As \[ I_{DS6} = I_{DS7} \]

\[ \left(\frac{W}{L}\right)_7 = \frac{I_{SD7}}{I_{SD6}} \left(\frac{W}{L}\right)_5 \] (5)

Step 6: Over all DC gain of the two stage is

\[ A = g_{m2} g_{m7} R_1 R_2 \]

\[ A = \frac{g_{m2} g_{m7}}{g_{DS2} + g_{DS4}} \left(\frac{g_{DS6} + g_{DS7}}{g_{DS5}}\right) \] (6)

Step 7: Flicker noise the transistor is given by

\[ v_{eq}^2 \quad f = \frac{K}{W L C_{OX}} \frac{1}{f} \]

Total input referred flicker noise at transistor M1

\[ v_{total}^2 = \frac{2K_p}{W L C_{OX} f} \left(1 + \frac{K_n \mu_n L_1^2}{K_p \mu_p L_3^2}\right) \] (7)

Where \( K_n \) an \( K_p \) is flicker noise co-efficient of nMOS and pMOS, depend on process parameter

Step 8: Total output swing

\[ V_{out\ swing} = V_{DD} - 4V_{DS} \] (8)

Table I presents the W/L ratios of all the transistors of the amplifier shown in Fig.2.(a), where M13,M14,M15 and M16 are drawn with narrow gate length and width to get required substrate biasing voltage.

<table>
<thead>
<tr>
<th>Transistor number</th>
<th>W/L (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M5,M6,M7,M8</td>
<td>0.5/0.5</td>
</tr>
<tr>
<td>M13,M14,M15,M16</td>
<td>1.8/0.18</td>
</tr>
<tr>
<td>M9,M10,M19,M20</td>
<td>2/0.5</td>
</tr>
<tr>
<td>M11,M2,M3,M4</td>
<td>81.26/0.5</td>
</tr>
<tr>
<td>M13,M14,M15,M16</td>
<td>5/0.5</td>
</tr>
<tr>
<td>M17,M18</td>
<td>1/0.5</td>
</tr>
<tr>
<td>M11,M12</td>
<td>13.61/0.5</td>
</tr>
</tbody>
</table>

III. SIMULATION AND RESULTS

The amplifier was designed using the transistor parameters of a TSMC 90nm CMOS process technology.

A. Closed Loop Gain Analysis

The new bio-amplifier achieves a 64dB gain with very good phase stability of 83°. Its -3dB bandwidth goes from 977.65 mHz to 10.1kHz and unity gain frequency 64 Mhz. The gain and phase profile is shown in Fig 3.

As far as noise is concerned, the simulation result showed that the output noise is constant and very low over the entire bandwidth. From noise profile of the amplifier shown in Fig 4, the output referred noise is of 8nV/√Hz and total input referred noise 28nV/√Hz at 1KHz frequency.
C. **Output Swing Analysis**

Sine wave inputs with amplitude levels of 250 mVpp is applied to the amplifier to evaluate the output swing. From the fig 5, it shows that output swing range 0.2-1V for 1V supply voltage. Beyond 250 mV amplitude of input neural signal, the output signal starts to clip of.

D. **Comparison with previous design**

The power and Noise profile of the four designs is shown in Fig 6. From the Fig 6 it is raveled that the our design consume smallest power about 91 μW. The input referred noise is appreciably lower about 28nV/√Hz.
IV. CONCLUSION

In this paper, we present the design approach and implementation of a Low power and low noise, rail-to-rail output swing Opamp. We discussed the basic theory behind the two stage operational amplifier. This is followed by a design procedure to get the most optimized performance for power consumption and noise. The output referred noise of 8nV /sq Hz makes this amplifier suitable for low-power Biopotential applications.

REFERENCES