Flip-flop and latches are used as data storage elements. Such data storage can be used for storage of state and such a circuit is described as sequential logic. The state of a latch or flip-flop is switched by a change in the control input. This momentary change is called a trigger and the transition it causes is said to trigger the flip-flop. Flip-flops can be either simple (transparent or opaque) or clocked (Synchronous or edge triggered). The simple ones are commonly called latches. The word latch is mainly used for storage elements, while clocked devices are described as flip-flops. A latch is level sensitive whereas a flip-flop is edge sensitive. When a latch is enabling it becomes transparent, while a flip-flops output changes on a single type of clock edge.

II. PROPOSED WORK

The D Flip-flop is the edge-triggered variant of the transparent latch. On the rising (usually, although negative edge triggering is just as possible) edge of the clock, the output is given the value of the D input at that moment. The output can be only change at the clock edge, and if the input changes at other times, the output will be unaffected.

D flip-flops are by far the most common type of flip-flops and some devices are made entirely from D flip-flops. They are commonly used for shift-registers and input synchronization.

Objectives

- reduce the power consumption.
- To reduce To the area.
- To reduce the delay and power of a clock network.
- To control clock skew because of common clock signal.

The above objectives can be achieved by merging several flip-flops and synchronizing with clock signals.

Problem Statement

The following problem statement has been identified:

- Several Flip-flops needs a separate clock signal, hence Power consumption, is high.
- Since several flip-flops needs a separate clock signal area consumed is also high.
III. BLOCK DIAGRAM AND ITS MODULES

This deals with the block diagram of the proposed method and its modules.

**Block Diagram**

The block diagram of the Application of Multi-bit flip-flop using QCL Adder as shown in figure 3.1

![Block Diagram]

**Fig 3.1 Block diagram of the application of Multi-bit flip-flop using QCL adder**

In the above block diagram, two inputs are given to QCL adder. QCL adder are developed by Majority Logic XOR, AND, OR gate. The output of QCL adder is fed to highest bit ‘1’ finding Algorithm. This Algorithm finds the number of bits and the combination table is built in order to merge the Flip-flops and it is stored in the Variable register banks.

**Modules**

This focuses on three different types of modules which are explained below.

- Design And Analysis Of Multi-Bit Flip-Flops
- Design Of Memory Device Using Multi-Bit Flip Flop
- Design and analysis of the Integration module

**Design And Analysis Of Multi-Bit Flip-Flops**

This module is used to reduce the power consumption by replacing some flip flop with fewer Multi-Bit flip flops. We are using the Multi-Bit flip flops instead of more single bit flip flop in order to increase the clock synchronisation. This will reduce the unnecessary power wastage through the use of multiple clock sinks.
Design of Memory Device Using Multi-Bit Flip Flop

This is the application module to be developed. The memory designed by mainly using the multi-bit flip flops. In this, power consumption of memory devices is reduced compare to the single bit memory.

Design And Analysis Of The Integration Module

We are integrating all the sub modules and output signals are simulated.

IV. RESULTS AND DISCUSSION

This we have merged the 1 bit and 2 bit flip flop to create the 4 bit and 8 bit flip flop, and using this default library is to create the other possible combinations. After that, introduce the application module as QCL adder using majority logic gates (majority AND, majority XOR and majority OR). The number of bits in the input of QCL adder is detected by using highest bit 1 finding algorithm. And depending upon the algorithm, the output value of QCL adder is stored in the merged flip flops, after looking the combination table. The merging of flip flop and using the highest bit 1 finding algorithm for storing the data in the flip flop reduce the power consumption.

Simulation Waveform:

We are using the Multi-Bit flip flops instead of more single bit flip flop in order to increase the clock synchronization. This will reduce the unnecessary power wastage through the use of multiple clock sinks.

Power consumption, are also reduced by replacing the Multi-Bit flip flop by gated multi-bit flip flop. In this we are using the AND gate as control device. This module is about the analysis of the power consumption of gated Multi-Bit flip flop with Multi-Bit flip flop.

REFERENCES