A Technique to Reduce Power Consumption Delay & Area in Wide Fan-In Domino OR Logic

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Abstract—In this paper, a new domino circuit is proposed, which has a lower leakage and higher noise immunity without dramatic speed degradation for wide fan-in gates. In this domino circuit a chain of evaluation network uses well known stacking effect technique to reduce the leakage. The stacking effect and current mirror makes the circuit more noise immune and considerably improves the Power Delay Product (PDP) as compared to the other existing domino logic. The leakage current is also decreased by exploiting the foot transistor in diode configuration, which results in increased noise immunity. DCLCR domino circuit reduces the leakage power consumption by maintaining the same level of delay. By connecting the gate of the transistor $M_{k1}$ to its drain power is reduced up to 14% as compare to standard footless domino and 24%. Simulation results of wide fan-in gates designed using a 65-nm high-performance predictive technology model (PTM) for 8 Input OR Logic.

Keywords—Domino logic; Evaluation Delay; Keeper transistor; Noise immunity; Wide fan-in gate.

I. INTRODUCTION

Dynamic logic such as domino logic is widely used in many applications to achieve high performance, which cannot be achieved with static logic styles [1]. However, the main drawback of dynamic logic families is that they are more sensitive to noise than static logic families. On the other hand, as the technology scales down, the supply voltage is reduced for low power, and the threshold voltage (Vth) is also scaled down to achieve high performance. Since reducing the threshold voltage exponentially increases the sub-threshold leakage current, reduction of leakage current and improving noise immunity are of major concern in robust and high-performance designs in recent technology generations, especially for wide fan-in dynamic gates. Less threshold voltage means smaller gate switching trip point in domino circuits. Smaller trip points make the domino circuit more prone to input noise. Moreover, excessive leakage can discharge the precharge (dynamic) node of a domino circuit resulting in a logic failure (wrong evaluation). In addition to reduced trip point and increased leakage, other noise sources such as supply noise and cross talk noise also increase by technology scaling, further degrading the robustness of domino logic [2–7].

A conventional approach to improve the robustness of domino circuits is keeper transistor upsizing. However, as the keeper transistor is upsized, the contention between keeper transistor and NMOS evaluation network increases in the evaluation phase. Such current contention increases evaluation delay of the circuit and increases power dissipation. Thus, keeper upsizing trades off delay and power to improve noise and leakage immunity. Such trade-off is not acceptable because it may make the circuit too slow or too power hungry. There are techniques proposed in the literature to address this issue. High speed domino logic [8] and conditional keeper [9] are among the most effective solutions for improving the robustness of domino logic [10–14]. In this paper, we propose a new domino circuit for high fan-in and high-speed applications in ultra-deep submicron technologies.

Keeper transistor upsizing is a conventional method to improve the robustness of domino circuit. A full keeper is added in precharge node to improve the robustness of the dynamic node. The keeper ratio ($K$) is defined as the ratio of the current drivability of the keeper transistor to that of the evaluation transistor,

$$K = \frac{\mu_p(W/L)^{\text{keeper transistor}}}{\mu_p(W/L)^{\text{evaluation transistor}}}$$

Where, $W$ and $L$ denote the transistor size, $\mu_p$ and $\mu_n$ are the mobility of electron and hole respectively.

As the keeper transistor is up-sized the contention between the keeper transistor and the evaluation network increases in the evaluation phase this causes an increase in the evaluation delay, power consumption of the circuit and degrading the performance [23]. To improve noise immunity and controlling the leakage, keeper upsizing is used as a compromise between delay and power. Therefore keeper upsizing may not be a viable solution for high leakage immunity problem in scaled domino circuit.
The paper is organized as follows. Literature review about existing domino circuit discussed in section 2. The proposed circuit description is in Section 3. Simulation result is presented and compared in section 4 with the brief conclusion of the paper in section 5.

II. LITERATURE REVIEW

Several domino circuits have been proposed in the literature such as conventional higher fan-in domino OR logic with footer less and footer transistor, high speed domino, conditional keeper domino, wide OR gate diode footer domino. The main goal of these circuit design technique is to improved Power consumption, Delay and Area for high circuit performance, especially for wide fan-in circuit.

2.1 Standard Footless Domino Logic Circuit (SFLDL)

The footless scheme [10] is characterized by the fact that discharge of dynamic node is faster. This property is exploited by the high-performance circuits. The circuit of the SFLD logic is shown in Fig 1. Operation of Footless-Domino is as follows:

Precharge phase: During the pre-charge phase, i.e. when then clock (CLK) is LOW, the dynamic node is charged to V_DD and the keeper transistor MP_2 turns ON to maintain the voltage of the dynamic node.

Evaluation phase: During the evaluation mode, i.e. when the CLK goes HIGH, the dynamic node is either discharged to ground or remains HIGH depending on the inputs. The size of the keeper transistor should be large enough to compensate for charge sharing problem and at the same time it should be small enough to reduce the contention between the keeper and the nMOS pull down transistor in the case the pull down network evaluates the dynamic node to logic level zero. Otherwise, the pull down network and keeper transistor compete to drive the dynamic node to two opposite directions, this effect is called contention and this results in the degradation of speed.

2.2 Standard Footed Domino Logic Circuit (SFDL)

The footer nMOS transistor MN_2 is connected to the source of evaluation nMOS transistor to obtain the FDL design which basically reduces the leakage current. The speed the SFDL is lower than the footless one because of the stacking effect [18], but the noise immunity is higher. Fig 2 shows the most conventional footed domino logic circuit. When clock is low, the dynamic node is precharged to V_DD [19]. In this phase the footed transistor MN_2 is turned off, which reduces the leakage current. When clock goes high, footer transistor MN_2 is turned on. So, depending on incoming data to pull-down network the state of output node is obtained.

Fig. 1. Standard Footless Domino Logic Circuit

Fig. 2. Standard Footed Domino logic circuit
2.3 High Speed Domino Logic (HS)

The circuit of the HS Domino logic is shown in Fig. 3 [19], [20]. In HS domino the keeper transistor is driven by a combination of the output node and a delayed clock. The circuit works as follows: At the start of the evaluation phase, when clock is high, MP3 turns on and then the keeper transistor MP2 turns OFF. In this way, the contention between evaluation network and keeper transistor is reduced by turning off the keeper transistor at the beginning of evaluation mode. After the delay equals the delay of two inverters, transistor MP3 turns off. At this moment, if the dynamic node has been discharged to ground, i.e. if any input goes high, the nMOS transistor MN1 remains OFF. Thus the voltage at the gate of the keeper goes to VDD-Vth and not VDD causing higher leakage current though the keeper transistor. On the other hand, if the dynamic node remains high during the evaluation phase (all inputs at “0”, standby mode), MN1 turns on and pulls the gate of the keeper transistor. Thus keeper transistor will turn on to keep the dynamic node high, fighting the effects of leakage.

When all the inputs are at low logic level, i.e. in standby mode, the dynamic node after the delays of two inverters remains high, in this condition the output node of NAND gate goes low, this causes the large keeper PK1 to be turned on. The large keeper is deployed after a delay for two inverters, to prevent erroneous discharge of the dynamic node when all inputs remain LOW. The small keeper PK2; however remain ON to compensate for charge leakage until PK1 is activated.

2.4 Conditional Keeper Domino Logic (CKD)

Conditional Keeper employs two keepers, small keeper and large keeper [21]. In this technique, the keeper device (PK) in conventional domino is divided into two smaller ones, PK1 and PK2. The keeper sizes are chosen such that PK=PK1+PK2 [22]. Such sizing insures the same level of leakage tolerance as the conventional gate but yet improving the speed.

The circuit works as follows: in pre-charge phase when clock is low, the pull-up transistor is on, so the dynamic node starts being charge up to VDD. At the beginning of evaluation phase when clock is high pre-charge transistors and large keeper PK1 are off.

2.5 Split Domino Logic (SDL)

As mentioned before, there are many parallel branches in a large fan-in dynamic OR gate. When the dynamic node voltage remains at VDD, the nMOS pull-down branches cause a large amount of leakage current. The propagation delay is increased due the large parasitic capacitive effect as this parasitic capacitance must be discharged to zero during evaluation. Split-domino is a very smart technique that by splitting the pull-down network into smaller groups improves the operation of the gate by using small size of keeper in both situations [22]. Therefore, in theory we need two keeper transistors with a width almost half as much as the conventional circuit. Fig.5 shows the 16-bit domino OR gate split in two. The circuit overhead is not as much as it might look, as there are two static inverters in the conventional domino circuit in place of two and three input NAND gates and besides they can be implemented using minimum size transistors. The circuit overhead is almost the same as the conditional keeper technique.
III. PROPOSED CIRCUIT

3.1 Diode Connected Leakage Current Replica (DCLCR)

In this proposed circuit we modify the LCR circuit [15]. In this circuit a current mirror circuit is added at the keeper of the standard footless domino logic as shown in Fig. 7. Transistor MK1 of the current mirror circuit is in diode connection, i.e. gate of this pMOS transistor is connected to the drain. By doing so both the gate and drain of the pMOS transistor is at potential voltage level of KPR. KPR voltage is equals to the potential of drain of MK1. This DCLCR circuit takes all the advantage of LCR domino circuit. In addition to these advantage DCLCR circuit reduces the power consumption. In precharge mode when the clock is at low level and at standby mode when all the inputs are at low level the dynamic node is charge up to VDD. During this precharge mode output is at low logic level which turns on the keeper transistor MK2 and it acts as a short circuit transistor. Now the drain of the MK1 is directly connected to the dynamic node and because of the diode connection configuration of this transistor drain voltage of M1 is also at the voltage level of dynamic node. High voltage of drain of M1 transistor reduces the leakage current at standby mode. In this way leakage power is reduced in this diode connected leakage current replica domino logic circuit.

IV. SIMULATION RESULTS AND ANALYSIS

The simulation of circuits is performed by using Spectre Cadence tool which includes following analysis

- Transient analysis
- Power analysis
- Delay analysis and
4.1 Transient Analysis

- Transient analysis shows a graph between inputs, outputs with respect to time axis. Fig.8 shows the waveform of inputs, outputs, clock and dynamic node voltage of 8 inputs OR gate based on Proposed circuit and based on DCLCR logic style respectively.

![Fig. 8 Simulation results of 8 inputs DCLCD based OR gate](image)

4.2 Results

4.1 Power and Delay Analysis

The Power dissipation is depends upon three factor (1) Supply Voltage (2) DC current (3) No of elements. Power in the circuit is measured by the voltage and current in each branch and power consumed by each element. is tabulated in Table 1.

![Fig.9 Layout Diagram of DCLCR](image)

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Logic style</th>
<th>8 INPUT</th>
<th>16 INPUT</th>
<th>8 INPUT</th>
<th>16 INPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>SFLD</td>
<td>13.102</td>
<td>18.435</td>
<td>2.601</td>
<td>4.251</td>
</tr>
<tr>
<td>2.</td>
<td>SFD</td>
<td>17.120</td>
<td>22.321</td>
<td>2.562</td>
<td>3.705</td>
</tr>
<tr>
<td>4.</td>
<td>HSD</td>
<td>13.541</td>
<td>18.32</td>
<td>5.143</td>
<td>8.012</td>
</tr>
<tr>
<td>5.</td>
<td>SDL</td>
<td>12.95</td>
<td>15.651</td>
<td>2.881</td>
<td>5.023</td>
</tr>
<tr>
<td>6.</td>
<td>DFD</td>
<td>53.6</td>
<td>48.20</td>
<td>10.88</td>
<td>11.94</td>
</tr>
<tr>
<td>7.</td>
<td>DCLCR</td>
<td>16.24</td>
<td>21.21</td>
<td>2.224</td>
<td>3.113</td>
</tr>
</tbody>
</table>

4.3 Area:

This is the Layout Diagram for area Calculation of

V. CONCLUSION

The leakage current of the evaluation network of dynamic gates was dramatically increased with technology scaling, especially in wide domino gates, yielding reduced noise immunity and increased power consumption. In this research work, two different domino logic are implemented, first is diode connected leakage current replica (DCLCR). DCLCR circuit takes all the advantage of leakage current replica and the novelty of the proposed circuit is that DCLCR domino circuit reduces the leakage power consumption by maintaining the same level of delay. By connecting the gate of the transistor $M_{K1}$ to its drain power is reduced up to 14% as compare to standard footless domino and 24%.
REFERENCES


