Design of Multi Level Converter for Interline Power Flow Controller with Variable Inputs in SIMULINK/MATLAB

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Abstract--The Interline Power Flow Controller (IPFC) a concept for the compensation and effective power flow management of multi-line transmission systems. In its general form, the IPFC employs two or more number of converters (VSC) with a common dc link, each to provide series compensation for a selected line of the transmission system. Because of the common dc link, any converter within the IPFC is able to transfer real power to any other and thereby facilitate reactive power transfer among the lines of the transmission system. Since each converter is also able to provide reactive power compensation, the IPFC is able to carry out an overall real and reactive power compensation of the total transmission system. This capability makes it possible to equalize both real and reactive power flow between the lines, transfer power from overloaded to under loaded lines, compensate against reactive voltage drops and the corresponding reactive line power, and to increase the effectiveness of the compensating system against dynamic disturbances. The paper explains the basic theory and operating characteristics of the five level inverter based IPFC with phasor diagrams, and simulated waveforms in SIMULINK/MATLAB

Keywords - AC transmission, FACTS, IPFC, line compensation, 5 level inverter, power flow controller, Series compensation, VSC.

Section I

I. INTRODUCTION

Flexible AC Transmission Systems (FACTS) based on either Voltage or Current Source converters (VSC/CSC) these can be used to control steady-state as well as dynamic/transient performance of the power system. Converter-based FACTS controllers when compared to conventional switched capacitor/reactor and thyristor - based FACTS controllers such as Static Var Compensator (SVC) and Thyristor-controlled Series Capacitor (TCSC) have the advantage of generating/absorbing reactive power without the use of ac capacitors and reactors.

In addition converter-based FACTS controllers are capable of independently controlling both active and reactive power flow in the power system. Series connected converter-based FACTS controllers include Static Synchronous Series Compensator (SSSC), Unified Power Flow Controller (UPFC) and Interline Power Flow Controller (IPFC). A SSSC is a series compensator with ability to operate in active/inductive modes to improve the system stability. The IPFC includes a Static Synchronous compensator (STATCOM) and a SSSC that share a common dc-link.

The IPFC consists of two or more SSSC with a common dc-link so, each SSSC contains a VSC that is in series with the transmission line through a coupling transformer, and injects a voltage with controllable magnitude and phase angle into the line. IPFCs provide independent control of reactive power of each individual line, while active power could be transferred via the dc-link between the compensated lines.

Section II

A. Inter line power flow controller

Generally, the Interline Power Flow Controller (IPFC) is a combination of two or more independently controllable static synchronous series compensators (SSSC) which are solid-state voltage source converters which inject an almost sinusoidal voltage at variable magnitude and couples via a common DC link as shown in fig.1 Conventionally series capacitive compensation fixed thyristor controlled or SSSC based is employed to increase the transmittable real power over a given line and to balance the loading of a normally Encountered multi-line transmission system at their dc terminals and connected to the ac systems through their series coupling transformers.
Fig. 1. IPFC model

With this scheme in addition to providing series reactive compensation, any converter can be controlled to supply active power to the common dc link from its own transmission line.

B. Operating principle and phasor diagram for interline power flow controller

For simplicity for explaining of 3 phase IPFC a single phase IPFC was taken. The IPFC (Fig. 2) is designed with a combination of the two series connected VSC which can inject a voltage with controllable magnitude and phase angle at the fundamental frequency, while DC link voltage maintained at a desired level. The common dc link is represented by a bidirectional link (P1r = P1pq = P2pq) for real power exchange between two voltage sources. Transmission line reactance represented by X1 has a sending end bus with voltage Phasor \( V_{1s} \) and a receiving end voltage Phasor \( V_{1r} \). The sending end voltage Phasor of Line 2, represented by reactance \( X_2 \), is \( V_{2s} \) and the receiving-end voltage Phasor is \( V_{2r} \). Simply, all the sending-end and receiving-end voltages are assumed to be constant with fixed amplitudes, \( V_{1s} = V_{1r} = V_{2s} = V_{2r} = 1pu \), and with fixed angles resulting in identical transmission angle \( s_1 = s_2 \) for the two systems. The two line impedances and the rating of the two compensating voltage sources are also assumed to be identical.

This means \( X_1 = X_2 \) and \( V_{1pqmax} = V_{2pqmax} \). Although in practice system 1 and system 2 could be likely different due to different transmission line voltage, impedance and angle. We assumed system 1 is arbitrarily selected to be the prime system for which free controllability of both real and reactive line power flow is stipulated to derive the constraints the free controllability of system 1 forces on the power flow control of system 2. A phasor diagram of system 1 illustrated in Figure 3 defines the relationship between \( V_{1s} \), \( V_{1r} \), \( V_{x1} \) (the voltage phasor across \( X_1 \)) and the inserted voltage phasor \( V_{1pq} \), with controllable magnitude and angle.

\( V_{1pq} \) is added to the sending end voltage \( V_{1self} = V_{1s} + V_{1pq} \). So \( V_{1self} - V_{1r} \), the difference sets the compensated voltage phasor or \( V_{x1} \) across reactance \( X_1 \). As angle is varied over its full 360 degree range, the end of phasor \( V_{1pq} \) moves along a circle with its center located at the end of phasor \( V_{1r} \). The area within this circle defines the operating range of phasor \( V_{1pq} \). Thus the line 1 can be compensated. The rotation with angle of phasor \( V_{1pq} \) modulates both the magnitude and the angle of phasor \( V_{x1} \) and, therefore, both the transmitted real power, \( P_{1r} \), and the reactive power, \( Q_{1r} \), vary with 1.

Fig. 3. PHASOR Diagram Of System

This process requires the voltage source representing Inverter 1 (\( V_{1pq} \)) to supply and absorb both reactive, \( Q_{1pq} \), and real, \( P_{1pq} \), power.

Section III

II. DESIGN OF FIVE LEVEL CONVERTER

By using modern power electronics more revolution came in power generation and transmission. In the area of conversion (from AC- DC or DC to AC) the ability to continuous vary in output voltage, frequency and amplitude by selecting the right device. And their control. The high level inverters generate the ac voltages by switching at different levels at high frequency with semiconductor devices. The waveforms generated the inverter is differ from the general sinusoidal waveform because of rectangular switching.
A. Three Phase 5 Level Inverter

The above fig shows the three phase five level inverter which consists of totally twenty four IGBTs for three legs (Each leg consists 8 IGBTs) which are protected by anti parallel diodes. These anti parallel diodes are working as snubber circuits for protecting the IGBTs. For simplicity in explaining the operation of three phase inverter single leg was taken, the construction of single leg and design of capacitor explained in next paragraphs.

One pole (or phase) of the five level inverter is shown in Fig.5, where two additional poles would be required for a three phase VSI. Each IGBT is equipped with average conducting diode and a diode clamp to ensure that the voltage across a single IGBT does not exceed the voltage cross the supply. The lower four IGBT require the complementary gating pulses of upper four IGBTs of the same number. That is if 43 is on, then 43' must be off. The gate logic to achieve the five voltage levels at the output Va is shown in Table 1.
B. Various Strategies for The Control Of The Output Of Five Level Inverter

Voltage and frequency were investigated on the basis of number --of IGBT switching’s per fundamental cycle and the distortion factor defined as the rms value of the harmonic voltages normalized to the maximum fundamental voltage and divided by the harmonic number.

<table>
<thead>
<tr>
<th>OUTP (V_{\alpha})</th>
<th>IGBT STATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>UT 0</td>
<td>I I I I I I I</td>
</tr>
<tr>
<td>+2E</td>
<td>1 1 1 1 1 0 0</td>
</tr>
<tr>
<td>+E</td>
<td>0 1 1 1 1 0 0</td>
</tr>
<tr>
<td>0</td>
<td>0 0 1 1 1 1 0</td>
</tr>
<tr>
<td>-E</td>
<td>0 0 0 1 1 1 1</td>
</tr>
<tr>
<td>-2E</td>
<td>0 0 0 0 1 1 1</td>
</tr>
</tbody>
</table>

All odd non-triple harmonics where considered. A low distortion factor implies low losses due to harmonic voltages and currents and a low torque ripple.

Both fundamental frequency switching of the IGBTS with variable dc link voltages, and PWM techniques with fixed dc link voltages were studied.

C. Fundamental Frequency Switching

Fundamental frequency switching requires each device to be switched on and off just once per cycle of the fundamental frequency output and produces the staircase type waveform of Fig.6. There are a number of degrees of freedom that can be employed in arriving fundamental frequency switching at an optimum type of output voltage waveform. If we switch to the intermediate voltage, +E at \( \alpha_1 \), and to the full voltage, +2E at \( \alpha_2 \), the Fourier coefficients of the output voltage are calculated as the simple sum of the coefficients of the two rectangular waves. From equation (2) we can derive the various control options for the output voltage; E can remain constant and the angles \( \alpha_1 \) and \( \alpha_2 \) varied to control the fundamental voltage and minimize the distortion factor.

The dc voltage \( E \) can vary to control the output voltage. The first option (pulse width control) works well over very small ranges of output voltage, but over a large range, the distortion factor becomes prohibitively large for most transmission line applications.

C. Capacitor voltages in the five level inverter

Refer Fig. 5 all the capacitors are assumed to be equal and initially charged to a voltage of +E. If a single dc voltage of 4E is supplied to the inverter, then at full positive or negative output voltage the capacitor currents will be zero. However at an intermediate output voltage, the output is clamped to the point +E and the current \( iL_2=iA \), the output current. Similarly, at zero voltage, \( iL_3=iA \) and at -E, \( iL_4=iA \). If we define these three states as \( S_2 \), \( S_3 \) and \( S_4 \) respectively, where \( S_2 \) is 1 only during the time that the inverter output is clamped to +E and is 0 at all other times, then the three currents can be defined as: \( iLN=Sn*A \) where \( n=1,2,3,4,…,n \). In order to maintain a constant dc link voltage, the current \( iL_2 \) must divide in the ratio 3:1 with \( iC1=0.75*iL2 \) and \( iC2=iC3=iC4=0.25*iL2 \). The capacitor currents for the other states can be calculated in a similar fashion to yield the following equations for the capacitor currents:

\[
\begin{align*}
  iC1 &= (0.75*S2 + 0.5*S3 + 0.25*S4)*iA \\
  iC2 &= (-0.25*S2 + 0.5*S3 + 0.25*S4)*iA \\
  iC3 &= (-0.25*S2 - 0.5*S3 + 0.25*S4)*iA \\
  iC4 &= (-0.25*S2 - 0.5*S3 - 0.75*S4)*iA \\
  iC1 &= 0.75*iL2 \\
  iC2 &= iC3 = iC4 = 0.25*iL2.
\end{align*}
\]

\[
H(n)=\frac{4}{n}\frac{1}{\cos(n\alpha_1 + \cos(n\alpha_2))} \quad (2)
\]

Where n=1, 3, 5, 7, 9, 11
A. Design of Inter Line Power Flow Controller in matlab/simulink

A. Control Scheme of IPFC

The above two figures shows the design of control scheme for two voltage source converters.

The IPFC is designed to maintain the impedance characteristic of the two transmission lines. The inter line power flow controller mainly consists two voltage source converters 1. Main converter (master) and second one is slave converter. Depending upon the power flow (if power transmits from line one to line two the converter1 will work as converter and converter two work as inverter and vice versa.

Design of control scheme for converter1

The converter 1 mainly consists the following parts

- compensator, alpha- beta to d-q converter and PWM generator.

The slave converter mainly consists of following parts.

DC voltage controller, balancing controller, reactance controller, PWM generator.

The major difference between the two control schemes are the dc voltage controller and (b) the balancing controller. Since the dc-link voltage is controlled by the slave system, the dc voltage controller and balancing the controller is no longer needed. However, here two control loops are required to regulate the d- and q-components in the synchronous reference frame in order to regulate both the reactance and resistance of the Line 1.

ii Pulse Generation For VSC 1

The Fig.9 shows the triggering pulse generation circuit for voltage source converter 1. It generates totally 24 pulses are generated these pulses are applied to the 24 IGBTS which are connected in three legs of VSC1

iii Pulse Generation For VSC2

The Fig.10 shows the triggering pulse generation circuit for voltage source converter 2. It generates totally 24 pulses these pulses are applied to the IGBTS which are connected in three legs of VSC 2.

B. Simulation Results

The simulated power system (Fig.9) modeled with Simulink/Mat lab, consists of two identical transmission systems. The controller in vsc1 is designed to compensate 0.4Pu transmission line reactance and 0.2 Pu resistance of transmission line. In vsc2 designed to control the DC voltage and kept it at constant position and compensate the reactance of 0.4Pu.
The system was designed in Mat Lab/Simulink with variable inputs at different time intervals. The output results are tabulated at different time intervals (from 0s-2.5s)

Fig.9 triggering pulse generator for vsc1 & Fig10. Triggering pulse generator for vsc1
C. Inter Line Power Flow Controller With Five Level Inverter In Matlab

Fig. 11. Single line diagram for inter line power flow controller

Fig. 12. Interline power flow controller in matlab/simulink
D. Simulation waveforms in MATLAB/SIMULINK

Fig13.a Injected Voltages for line1 and 2

Fig13.b Injected currents for line and 2

Fig13.c Injected active and reactive powers for line1

Fig13.d Injected active and reactive powers for line 2

Fig13.e Voltage across capacitor (vdc)
Table 2. sending and receiving end powers

<table>
<thead>
<tr>
<th>S.NO</th>
<th>Real and reactive power analysis for line 1 and 2 (sending end and receiving end)</th>
<th>0-0.1s</th>
<th>0.1-0.2s</th>
<th>0.2-0.3s</th>
<th>0.3-0.4s</th>
<th>0.4-0.5s</th>
<th>0.5-0.6s</th>
<th>0.6-0.8s</th>
<th>0.8-1.0s</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>LINE 1 REAL POWER SENDING END (W)</td>
<td>1.1478 X10^8</td>
<td>1.3773 X10^8</td>
<td>1.1478 X10^8</td>
<td>1.1478 X10^8</td>
<td>1.1478 X10^8</td>
<td>1.1478 X10^8</td>
<td>1.1478 X10^8</td>
<td>1.1478 X10^8</td>
</tr>
<tr>
<td>2</td>
<td>LINE 1 REACTIVE POWER SENDING END ((-Ve) VAR)</td>
<td>0.765 X10^8</td>
<td>0.9155 X10^8</td>
<td>0.765 X10^8</td>
<td>0.765 X10^8</td>
<td>0.765 X10^8</td>
<td>0.765 X10^8</td>
<td>0.765 X10^8</td>
<td>0.765 X10^8</td>
</tr>
<tr>
<td>3</td>
<td>LINE 1 REAL POWER RECEIVING END (W)</td>
<td>1.4348 X10^8</td>
<td>1.4348 X10^8</td>
<td>1.81732 X10^8</td>
<td>1.81732 X10^8</td>
<td>1.4348 X10^8</td>
<td>1.4348 X10^8</td>
<td>1.4348 X10^8</td>
<td>1.4348 X10^8</td>
</tr>
<tr>
<td>4</td>
<td>LINE 1 REACTIVE POWER RECEIVING END ((-Ve) VAR)</td>
<td>0.9565 X10^8</td>
<td>0.9565 X10^8</td>
<td>1.1955 X10^8</td>
<td>1.1955 X10^8</td>
<td>0.9565 X10^8</td>
<td>0.9565 X10^8</td>
<td>0.9565 X10^8</td>
<td>0.9565 X10^8</td>
</tr>
<tr>
<td>5</td>
<td>LINE 2 REAL POWER SENDING END (W)</td>
<td>1.1478 X10^8</td>
<td>1.1478 X10^8</td>
<td>1.1478 X10^8</td>
<td>1.721 X10^8</td>
<td>1.1478 X10^8</td>
<td>1.1478 X10^8</td>
<td>1.81732 X10^8</td>
<td>1.1478 X10^8</td>
</tr>
<tr>
<td>6</td>
<td>LINE 2 REACTIVE POWER SENDING END ((-Ve) VAR)</td>
<td>0.765 X10^8</td>
<td>0.765 X10^8</td>
<td>0.765 X10^8</td>
<td>1.1478 X10^8</td>
<td>0.765 X10^8</td>
<td>0.765 X10^8</td>
<td>1.1956 X10^8</td>
<td>0.765 X10^8</td>
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<td>7</td>
<td>LINE 2 REAL POWER RECEIVING END (W)</td>
<td>1.4348 X10^8</td>
<td>1.4348 X10^8</td>
<td>1.4348 X10^8</td>
<td>1.4348 X10^8</td>
<td>1.4348 X10^8</td>
<td>1.4348 X10^8</td>
<td>1.81732 X10^8</td>
<td>1.4348 X10^8</td>
</tr>
<tr>
<td>8</td>
<td>REAL LOAD AT RECEIVING END LINE 1,2</td>
<td>190 MW</td>
<td>190 MW</td>
<td>150 MW</td>
<td>150 MW</td>
<td>190 MW</td>
<td>190 MW</td>
<td>190 MW</td>
<td>190 MW</td>
</tr>
<tr>
<td>9</td>
<td>REACTIVE LOAD AT RECEIVING END LINE 1,2</td>
<td>125 MVAR</td>
<td>125 MVAR</td>
<td>125 MVAR</td>
<td>125 MVAR</td>
<td>125 MVAR</td>
<td>125 MVAR</td>
<td>125 MVAR</td>
<td>125 MVAR</td>
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</table>

V. CONCLUSION

The design of an IPFC with five level inverter has presented in this paper. Two different control circuits were designed for generating triggering pulses for five level inverters. The IPFC system with two 5-level in MATLAB/SIMULINK was designed and results validated. The simulation waveforms presented in the paper. The real and reactive powers at sending end and receiving end at different levels are calculated and tabulated.

REFERENCES


