Comparison of CNTFET based 6T SRAM and MOSFET based 6T SRAM using Hspice.

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Abstract—The basic VLSI (Very Large Scale Integration) circuit element is Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Moore’s law states that, design performance improves by reduction in gate length. The gate length reduction is also known as scaling. The continuous scaling of the circuit design will cause issues related to electrical performance of the chip. The device fabrication creates major problems when the geometry reaches to nanometer region. For the same purpose, the researchers have found Carbon Nano-Tubes (CNT) as the new worthy candidate. The design of CNT defines its properties, either metallic conductor or semiconductor. The transistor made from CNT is referred as CNT Field Effect Transistor (CNTFET). In this paper, we have drawn comparison of 6T SRAM between MOSFETs and CNTFETs. Section-1 gives brief introduction of MOSFETs and CNTFETs whereas section-2 describes the detailed properties of CNTFETs and section-3 gives details about CNTFET model. Section-4 describes the detailed description about 6T SRAM Section-5 gives simulation results of 6T SRAM. Section-6 summarizes the paper and shows future prospects of CNTFETs’ usage.

Keywords— CNTFET, MOSFET, Chirality, Graphene, 6T SRAM

I. INTRODUCTION

For many years, VLSI chip designers have been using metal-oxide semiconductor field-effect transistors (MOSFETs) as basic circuit elements. Designers have used MOSFET based circuits in their designs because they consume lesser power and are cheaper to fabricate [1-2]. The VLSI designs demands high chip density, high speed and low power. These essencials can be achieved by reducing the size of transistor, a process known as scaling [3]. The continuous scaling of the circuit design gives rise to problems like; short channel effect, power dissipation, leakage current and process variation [2, 5]. As a solution to correct these shortcomings and achieve similar performance; the CNTFET is explored. They can be tailor designed to overcome the difficulties encountered during MOSFET scaling [6]. CNT is manufactured with a sheet of graphene rolled up into a cylindrical structure. The CNT can work as metal or semiconductor, based on how the sheet is rolled up [13]. The graphene rolling is expressed by roll vectors (n, m) values, described in section-3.

The CNT based FETs can achieve the performance like traditional MOSFET. Prior to the comparison, one must first assume that the CNTFET resemble their characteristics with MOSFET [5, 14-15]. There are prevailing problems related to the CNTFETs’ manufacturing yield. The MOSFET based technology is matured and hence are not detailed as fabrication aspects but, their electrical characteristics are discussed extensively.

II. CNTFET

Carbon is a Group 14 element that resides above silicon in the Periodic Table. Like silicon and germanium, carbon has four electrons in its valence shell. When carbon atoms are arranged in crystalline structures (composed of hexagonal benzene - like rings), they form a number of allotropes that offer exceptional electrical properties [4, 11].

Figure-1 Graphene atomic structure with a translational vector T and a chiral vector C of a CNT

In their semiconducting forms, this carbon nano-material exhibit room-temperature mobility more than ten times greater than silicon [4]. In addition, they can be scaled to smaller feature sizes than silicon while maintaining their electrical properties [4, 13]. Carbon nanotube (CNT) was discovered by S. Ijima in 1991 [6, 8, 11-12, 13, 17-19]. CNTs are hollow cylinders, composed of one or more concentric layers of carbon atoms (graphene) in a honey comb lattice arrangement [4, 13, 18, 20].
The way in which graphene is rolled is expressed by a pair of indices \((n, m)\) called “chiral vector” [7, 10, 14, 16, 20, 21, 24].

\[
C = n_1 a_1 + n_2 a_2
\]

Where \(a_1\) and \(a_2\) are unit vectors [4][13].

The figure-1 illustrates the basic construction of CNT from graphene (which look like as honey bees’ area). The CNTFET uses conducting channel of CNT between source and drain regions.

CNTFET Basic Parametric Equations:

The single-walled CNT (SWCNT) is treated as a quasi-1-D quantum wire in this paper. For SWCNT with chirality \((n_1, n_2)\), the diameter \((D_{CNT})\) is given by \((a = 2.49 \, \text{Å} \text{ is the lattice constant})\) [16, 24, 25].

\[
D_{CNT} = \frac{a\sqrt{n_1^2 + n_2^2 + n_1 n_2}}{\pi}
\]

Depending on the shape of the cross-section established by the chiral vector slicing across the hexagonal pattern, nanotubes are classified in one of the three groups as: armchair \((n_1 = n_2\) and \(\zeta=30º)\), Zigzag \((n_2=0 \text{ and } \zeta=0º)\), and chiral (all other cases) where \(\zeta\) is the angle between chiral vector \(C\) and zigzag direction vector. Figure-2 shows all these three types of CNTs [10, 20]. As in [27], \((m, l)\) is the \(l\) th substate at the \(m\) th subband, \(k_m\) is the wavenumber of the \(m\) th subband in the circumferential direction, and \(k_l\) is the wavenumber of the \(l\) th substate in the current-flow direction. It defines the subbands with positive band gap as “semiconducting subbands,” and the subbands with zero or negative band gap as “metallic subbands.” Thus, the band structure of metallic nanotubes can be treated as a summation of the metallic and semiconducting subbands. The wave numbers related with semiconducting subbands are given by,

\[
k_m = \frac{2\pi \lambda}{a\sqrt{n_1^2 + n_2^2 + n_1 n_2}}
\]

\[
\lambda = \begin{cases} 
\frac{6m - 3 - (-1)^m}{12}, & m = 1, 2, \ldots \\
\text{mod}(n_1 - n_2, 3) \neq 0 & m = 0, 1, \ldots \\
\text{mod}(n_1 - n_2, 3) = 0 
\end{cases}
\]

\[
k_l = \frac{2\pi}{L_g} l
\]

The energy of the \((m, n)\) th sub-band, above \(E_i\) is

\[
E_{m,i} \approx \frac{\sqrt{3}}{2} a V_\pi \sqrt{k_m^2 + k_l^2}
\]

Here, \(V_\pi\) is the carbon \(\pi-\pi\) bond energy in the tight bonding model; \(-3.033\, \text{eV}\). There are three current sources in the CNFET model: 1) the thermionic current contributed by the semiconducting subbands \(I_{semi}\) with the classical band theory; 2) the current contributed by the metallic subbands \(I_{metal}\); and 3) the leakage current \(I_{btbt}\) caused by the band-to-band tunneling (BTBT) mechanism through the semiconducting subbands. In the subthreshold region, particularly with negative gate bias (nFET), the \(I_{btbt}\) from drain to source becomes significant.

\[
I_{btbt} = \frac{4e}{h} kT \sum_{k_m}^{M} \left[ T_{btbt} \ln \left( \frac{1+e^{\frac{eV_{ch,DS}-E_{m,0}-E_f}{kT}}}{1+e^{\frac{eV_{ch,DS}-E_{m,0}}{kT}}} \right) \right] \times \max\left(\frac{eV_{ch,DS}-E_{m,0}-E_f}{eV_{ch,DS}-2E_{m,0}}\right)
\]

Here, \(k\) is the Boltzmann constant, \(T\) is the temperature in Kelvin, \(E_{m,0}\) is the half band gap of the \(m\) th sub-band, \(V_{ch,DS}\) is the Fermi potential differences near source side within the channel, \(e\) is the unit electrical charge and \(E_f\) is fermi level of doped source/drain nanotube in electron-volt (ev). \(T_{btbt}\) is defined as the Wentzel–Kramers–Brillouin-like transmission coefficient [27, 28] and it is given by

\[
T_{btbt} \approx \frac{\pi^2}{9} \exp\left(-\frac{\sqrt{m}^{(1/2)}(\sqrt{2}mE_{m,0})^{3/2}}{2^{7/2}e.\text{h.E}}\right)
\]
Where $\eta_m$ is a fitting parameter, which represents the band-gap narrowing effect under high electrical field [25] [26], $F$ is the electrical field triggering the tunneling process near the drain side junction.

III. DESCRIPTION ABOUT CNTFET MODEL

As explained previously, CNTFET can even work as a semi conducting device. There are mainly two types of CNTFET: (a) Schottky barrier CNTFET (SB-CNTFET) and (b) MOSFET like CNTFET. Figure 3(a) shows the structure of SB-CNTFET, where the channel is made up of intrinsic semiconducting CNT in direct metal contact with source and drain regions. The device works on the principle of direct tunneling through the Schottky barrier (SB) at the source-channel junction. The barrier-width is modulated by the application of gate voltage, and hence, the transconductance of the device is controlled by the gate voltage. Figure 3(b) shows three dimensional device structure of MOSFET-like CNFET with multiple channels, high-k gate dielectric material, and related parasitic gate capacitances. It shows three CNFETs are fabricated along one single CNT [31, 32]. The channel region of CNTs is undoped, whereas the other regions of CNTs are heavily doped. The figure 3(b) shows the 3-D device structure of CNFET that is modeled in this paper, with only the intrinsic channel region.

This section gives comparison between traditional MOSFET and CNTFET for I-V (P-channel and N-channel) characteristics and Voltage Transfer Characteristics (VTC). The comparison is carried out on the 32nm technology models. The MOSFET and CNTFET HSPICE models are selected from [22] and 32nm BSIM PTM (Predictive Technology Model) Si-MOSFET, respectively. The CNTFET model works for MOSFET like CNFET device. It models voltage controlled current source $I_{bsb}$ in order to evaluate the device sub-threshold behaviour and the static power consumption. The expression for $I_{bsb}$ is given in earlier section. The simulation is carried out using HSPICE. This tool is used for simulation because it has capability to incorporate custom (CNTFET) library, various functions availability, data analysis capability, data display in tabular form, measurement analysis etc. To view output of simulations we have used Wave View tool of Synopsys. Each of the devices (P-MOSFET, N-MOSFET, N-CNTFET, and P-CNTFET) is simulated with single run and recorded.

IV. DESCRIPTION ABOUT 6T SRAM

Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. This storage cell has two stable states which are used to denote “0” and “1”. Two additional access transistors help controlling the access to the cross coupled unit formed by the inverters during read and write operations.
So typically it takes six transistors to store one memory bit. The design of a basic SRAM cell is shown in Figure 5. Access to the cell is enabled by the word line (WL) which controls the two access transistors M5 and M6 which allow the access of the memory cell to the bit lines: ‘BL’ and ‘BLbar’. They are used to transfer data for both read and write operations. The presence of dual bit lines i.e. ‘BL’ and ‘BLbar’ improves noise margins over a single bit line. The operation of CNFETs based memories is very similar to that of CMOS except for minor differences in device orientation. One such difference being that the source and drain terminals of a CNFET are not interchangeable as is the case with CMOS devices. Care must therefore be taken to orient the transistors in a memory cell in a manner that will ensure correct transmission of logic levels.

**Write Operation:**

The start of a write cycle begins by applying the value to be written and its complement to the bit lines. In order to write a ‘0’, we would apply a ‘0’ to the bit line ‘BL’ and its complement ‘1’ to the ‘BLbar’. A ‘1’ is written by inverting the values of the bit lines i.e. by setting ‘BL’ to ‘1’ and ‘BLbar’ to ‘0’. ‘WL’ is then made high and the value that is to be stored is latched in. The input drivers of the bit lines are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross-coupled inverters. Proper operation of an SRAM cell however needs careful sizing of the transistors in the unit.

**Read Operation:**

The read cycle is started by asserting the word line ‘WL’, enabling both the access transistors M5 and M6. The second step occurs when the values stored in ‘Q’ and ‘Qbar’ are transferred to the bit lines ‘BL’ and ‘BLbar’ through M1 and M6. On the BL side, the transistors M4 and M5 pull the bit line towards VDD (when a “1” is stored at Q). If the content of the memory was a 0, the reverse would happen and ‘BLbar’ would be pulled towards 1 and ‘BL’ towards 0.

**Idle State:**

For the idle state, the word line is not asserted and the access transistors M5 and M6 disconnect the cell from the bit lines. The two cross coupled inverters INV1 and INV2 formed by M1, M2 and M3 M4 will continue to reinforce each other as long as they are disconnected from any external circuits.

<table>
<thead>
<tr>
<th>DATA</th>
<th>ENABLE</th>
<th>WORD LINE</th>
<th>BIT LINE</th>
<th>OUTPUT DATA</th>
<th>STATUS</th>
</tr>
</thead>
<tbody>
<tr>
<td>*</td>
<td>0</td>
<td>0</td>
<td>Z</td>
<td>DATA</td>
<td>STORE</td>
</tr>
<tr>
<td>*</td>
<td>0</td>
<td>1</td>
<td>DATA</td>
<td>DATA</td>
<td>READ</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>DATA</td>
<td>STORE</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>DATA</td>
<td>STORE</td>
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<tr>
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<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>WRITE 0</td>
</tr>
<tr>
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<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>WRITE 1</td>
</tr>
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Table-2 Write and Read operation for Data 0 and 1.

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<th>write (0) and read 0 operation</th>
<th>WR-0</th>
<th>ST</th>
<th>ST</th>
<th>ST</th>
<th>RD</th>
</tr>
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<tbody>
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<td>1</td>
<td>0</td>
<td>0</td>
</tr>
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<td>WL</td>
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<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
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<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>BL</td>
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<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
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<td>1</td>
<td>1</td>
</tr>
<tr>
<td>BL2</td>
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<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>BLR2</td>
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<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>write (1) and read (1) operation</th>
<th>WR-1</th>
<th>ST</th>
<th>ST</th>
<th>RD</th>
</tr>
</thead>
<tbody>
<tr>
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<td>1</td>
<td>0</td>
<td>0</td>
</tr>
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<td>1</td>
</tr>
<tr>
<td>DT</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>BL</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
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<tr>
<td>BL2</td>
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<td>1</td>
</tr>
<tr>
<td>BLR2</td>
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<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Figure-5 Simulation Results for 6T SRAM Using MOSFET

VI. CONCLUSION AND FUTURE WORK

Unipolar, MOSFET-like CNTFET model is used to implement 6T SRAM. This model is used for designing 6T SRAM circuits whose coding has been done in HSPICE, the output waveform is displayed on AvanWaves and delay, average power calculations have been done for these circuits for the value of supply 0.6 V. Implementation of 6T SRAM simulation using MOSFET and CNTFET is compared. Performance using CNTFET model is better than the MOSFET based design.

REFERENCES


