Development and Analysis of VHDL Architecture of Reconfigurable Digital Modulator and Demodulator

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Abstract— In this paper, the VHDL design and implementation of BPSK, BASK and BFSK modulator and demodulator with mixed domain performance analysis under different software are presented. The modulators are widely used in communication system either wired or wireless also the applications of these devices are ranging from personal to industrial. Because the every techniques has their own advantages and disadvantages and hence designer chooses the best depending upon the applications requirement this creates the problem for the applications with time changing requirements. The design presented in this paper provides a solution for such cases by providing simple programmable interface for switching among different techniques with low power and FPGA resource consumption also the proposed design architecture maintains the simplicity without compromising the performance and through simulation we check that with the considerable gain in signal to noise ratio (SNR) and there is minimization of bit error rate (BER). Final the design is synthesizes using Xilinx software and because the performance analysis under application domain which contains several analog variables is not possible with Xilinx the system is also analyzed in Matlab/Simulink software and the measured results shows that the proposed design architecture provides expected results furthermore the analysis results can be used in field for choosing the correct device to properly match the requirements.

Keywords— Digital Modulators, BPSK, BASK, BFSK, Communication channel.

I. INTRODUCTION

Wireless communication is one of the most common areas in communication field, because of increased demand for connectivity which is mainly established by wired and wireless data communication systems. Since every communication systems is aimed to get high data transmission rate for efficient transmission of information and maximum utilization of the available channel bandwidth. Although every section from error correcting codes to transmission antenna contribute to achieve this and one of these section is modulator, because modulation techniques enables system to improve data transmission rate within the same available channel bandwidth.

Hence the modulator can provide sufficient transmission rate gain but it requires flexible and configurable architecture to withstand with varying channel conditions because the efficiency of modulation technique also depends upon channel conditions.

Looking on the hardware aspects the Field-programmable gate arrays (FPGAs) is one of the recently developed advance semiconductor devices. The FPGA contains programmable logic elements (LEs) and reconfigurable interconnects to form complex combinational and/or sequential logic functions. To use it as a specific hardware the FPGA can be configured by programming which forms the interconnections of logic elements for programmed applications, even after the product installation in the field.

To utilizing the capability of FPGA and the requirements of modulator a combined approach is used in this paper to provide the efficient solution. The rest of the paper is organized as, the second section provides a brief discussion of the most recent and relative literatures followed by a basic review of modulation techniques and channel impacts, in third and fourth section respectively. The fifth section explains the proposed algorithm and the simulated results are shown in the sixth section while the conclusion and future work on the basis of the simulation results is presented in seventh section.

II. LITERATURE REVIEW

This section presents a brief review of some of the most recent literature published in the related field. Santa Concepcion Huerta et al [1] proposed DPWM (Digital Pulse Width Modulator) which combines a synchronous (counter-based) block with an asynchronous block to increase the resolution without increasing the clock frequency and their proposed DPWM provides a final time resolution under 2 ns for an external 32 MHz clock.

Asraf Mohamed Moubark et al [4], published a study to develop an implementable low power QPSK modulator. The proposed technique uses lookup table inside a memory block to produce a modulated symbol according to the input data.
Juha Suviola et al [6] proposed a real time implementation of FPGA based frequency synthesizer by utilizing I/Q modulation. The core structure of the systems designed around digitally synthesized programmable low-frequency I/Q tone which is then moved to the required radio frequency range using I/Q modulation. The design is specifically emphasizes in the adaptive digital pre-distortion and calibration mechanisms which improve the limited sideband attenuation with local oscillator leakage of practical I/Q modulators. A shuffled iterative bit interleaved coded modulation (BICM) receiver is presented in [7]. A development of a wideband delta sigma modulator for completely digital UHF transmitters [9]. The complete digital architecture of the transmitter provides a promising solution for software defined radio (SDR) devices and applications. The proposed fully digital transmitter consists of three main units) 1) delta-sigma modulator, 2) high speed multiplexer and 3) switching-mode power amplifier.

Eric Monmasson et al [10], presented a study on FPGAs applications in industrial control, the literature starts with addressing different research fields where FPGAs are useful. Then features and capability of these devices are presented followed by their corresponding design and development tools. To show the advantages of using FPGAs in complex control applications, a sensor-less motor controller based on the Extended Kalman Filter has been demonstrated. Its development has been done to explain and discuss a dedicated design methodology. Another example of Artificial Neural Network Systems with some case studies are also presented to show the applicability of FPGAs in this field. Multi-Bit Sigma Delta Pulse-Width Modulator is presented by Zdravko Luki et al [3]. The key components of the presented controller are 1) new digital pulse-width modulator (DPWM), using multi-bit sigma-delta concept, and 2) dual-sampling mode PID compensator. The conditions in the converter circuit, decides the output voltage to either sample at a frequency lower than the switching frequency or at the switching rate. The steady-state condition uses under sampling to minimize the power consumption of the controller while occurring transients, to get instantaneous dynamic response, the controller samples at higher sampling rate.

III. DIGITAL MODULATORS

In electronics and telecommunications, modulation is considered as a method of varying/changing one or more properties of a periodic waveform, called as carrier signal (high frequency signal), employing a modulating signal that generally contains information to be transmitted. In digital modulation technique, an analog carrier signal is modulated by a discrete signal (Finite Value Signals). The variation/changes in the carrier signal are chosen from a finite number of ‘m’ alternative symbols (the modulation symbols).

The three most fundamental digital modulation techniques are:

- **PSK (Phase-Shift Keying):** finite numbers of carrier phase variations are used.
- **FSK (frequency-shift keying):** finite numbers of carrier frequency variations are used.
- **ASK (amplitude-shift keying):** finite numbers of carrier amplitude variations are used.

3.1 BPSK

BPSK is the simplest form of phase shift keying (PSK). It uses two phases which are separated by 180° and so can also be called as 2-PSK. It hardly matters exactly where the constellation points are positioned in this method, here in the Figure 1, waveform are shown on the real axis, at 0° and 180°.

![Figure 1: Waveform for different modulation techniques.](image)

3.2 FSK

Frequency-Shift Keying (FSK) is a process of modulating frequency property of carrier wave, where digital data is transmitted through discrete frequency changes of a carrier wave (figure 1). The simplest form of FSK is Binary-FSK (BFSK) which uses a pair of discrete frequencies to transmit binary (0s and 1s) information.
3.3 ASK

Amplitude-Shift Keying (ASK) is a process of amplitude modulation that represents digital data transmission as varying the amplitude of a carrier wave. In this system, the binary data 1 is represented by transmitting a fixed-amplitude carrier wave having fixed frequency for a bit duration of T seconds (figure 1). If the binary signal value is 1, then the carrier signal will be transmitted else a signal value of 0 will be transmitted.

IV. AWGN CHANNEL

Additive white Gaussian noise (AWGN) is a fundamental noise model employed in Information theory to mimic the effect of many random processes that occur in nature. The modifiers denote specific characteristics:

- 'Additive' termed because it is added to any noise that might be intrinsic to the information system.
- 'White' refers to concept that it has uniform power across the frequency band for the information system. It is an analogy to the color white which has uniform emissions at all frequencies within the visible spectrum.
- 'Gaussian' termed because it has a normal distribution in the time domain with an average time domain value of zero.

The wideband noise comes from several natural sources, like thermal vibrations of atoms in conductors (referred as thermal noise or as Johnson-Nyquist noise) shot noise, black body radiation from the earth and other warm objects, and from celestial sources like Sun. The central limit theorem of probability theory indicates that the summation of several random processes will tend to have distribution known as Gaussian or Normal.

AWGN is usually used as a channel model in which the only impairment to communication is a linear addition of wideband or white noise with a constant spectral density (expressed as watts per hertz of bandwidth) and a Gaussian distribution of amplitude. This model does not account for fading, frequency selectivity, interference, nonlinearity or dispersion. However, it produces simple and tractable mathematical models that are useful for gaining insight into the underlying behavior of a system before these other phenomena are considered.

V. PROPOSED METHOD

As shown in the Figure 2, the proposed unit contains five memory blocks of 8x256 bytes which produces the sine waves at different amplitude, frequency and phases, with 256 quantization levels.

The two bit command line is used to select the particular modulation technique however the same demodulator works for all type of modulations. The first block is common for all modulators while the second block is selected on the basis of command input. The output frequency of the carrier depends upon the recall rate of the memory address counter hence the carrier frequency can be easily adjusted to the required one.

For the demodulation the fifth memory block is used which is converted into square wave by comparing with a constant (128, since the wave amplitude is varied from 0 to 255 which avoids the signed and floating point computation). The XOR gate in the next stage with not works as XNOR hence produces the ‘1’ at the output for equal received and the locally generated carrier while produces ‘0’ for unequal inputs. This signal is the converted to bipolar signal which is required for proper operation of integrator. The integrator is forced to reset once in every cycle to avoid miss detection. Finally the output of integrator is passed through the comparator to detect and generate the binary demodulated output signal. Here, a block for bit error rate calculation can also be added for specific noise and for different modulation schemes.
In this model we provide interfacing between matlab/Simulink and VHDL (Xilinx ISE), simulated and verified the output waveforms of different modulations scheme in analog form. Figure 3 shows RTL of the proposed Digital Modulator and Demodulators. Whereas remaining Figures 4,5 and 6 shows its internal view and device utilization.
VI. RESULT

The proposed model shown in Fig. 2 has been verified by the means of a mixed-signal simulation. Simulation Result is shown in Fig. 7 in which, output waveform from the Xilinx Simulator showing different Modulation and demodulation. The top most waveform shows the output of the integrator, Out2 presents the output of the demodulator, Out1 shows the ASK, FSK and FSK modulated output waveform according to the modulation technique selected by cmd_0 and cmd_1 combinations; for the input data stream at input of data_in.

And Experimental Result has shown in Figure. 8 in which, graph of $E_b/N_0$ (energy per bit to noise power spectral density ratio) Vs BER (bit error rate). $E_b/N_0$ is an important parameter in digital communication, it is a normalized signal-to-noise ratio measure, also known as the "SNR per bit". Proposed design is useful to compare BER performance of different digital modulation schemes without taking bandwidth into account. Result shows, As the SNR increase, BER constantly decreases proving the system to be efficient. BER of PSK is lesser for SNR than the other ASK and FSK modulation techniques.

VII. CONCLUSION

This paper presents an efficient architecture of the reconfigurable digital modulator and demodulator which can be configured for one of the techniques from BPSK, BFSK and BASK, using two bit bus interface, also the design uses only single demodulator for demodulating every type of modulation hence saves FPGA space and resources. The simulation also shows that the proposed design provides efficient performance under noisy environments. Furthermore the paper also presents the analysis of the proposed technique in Matlab/Simulink environment to extensively test its performance under practical operating environment the results from the Matlab also verifies the effectiveness of the proposed design.

REFERENCES

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[10] Eric Monmasson, Senior Member IEEE, Lahoucine Idkhajine, Marcian N. Cirstea, Senior Member, IEEE, Imene Bahri, Student Member, IEEE, Alin Tisan, Member, IEEE, and Mohamed Wissem Naouar, Member, IEEE “FPGAs in Industrial Control Applications”


[12] Anshul Agarwal, Student Member, IEEE and Vineeta Agarwal, Senior Member, IEEE “FPGA Realization of Trapezoidal PWM for Generalized Frequency Converter”
