Design and Comparative Analysis of EEAL Sequential Circuit for Low Power VLSI Application

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Abstract—A new design of adiabatic circuit, called Energy Efficient Adiabatic Logic (EEAL) is proposed \cite{1}. In adiabatic logic, which dissipates less power than static CMOS logic, have been adiabatic circuits called energy efficient adiabatic logic introduced as a promising new approach in low power circuit design \cite{2}. In this paper, my primary aim is to improve power delay product (PDP) of the proposed adiabatic circuits as compared with conventional CMOS circuits. In this paper work, we use two phase split level sinusoidal power supply which is used for low power high speed adiabatic circuits and diode is replaced by MOS transistor at charging and discharging path whose gate is controlled by power clock. By using this technique power dissipation of the diode is eliminated. In this paper we have designed and simulated EEAL Based Master-Slave JK Flip Flop, and EEAL Based 3-bit Counter. All the simulation in this paper have been implemented by VIRTUOSO SPECTRE simulator of cadence with the 0.18 micrometer UMC technology MOS transistor model under 1.8- volts peak to peak split level sinusoidal power clock supply. From the simulation result, we have find that proposed logic circuits can save significant amount of energy compared to CMOS.

Keywords—Low power adiabatic logic, Energy Efficient, Flip-flop, Counter, Power Dissipation

I. INTRODUCTION

In modern applications, like portable devices, energy has become an important concern: as end users require smaller devices with longer battery life, energy dissipation and fabrication space can be considered as critical concern. The main source of power dissipation in digital circuits is the dynamic power. Several methods to reduce the power dissipation have been reported. One of the methods to reduce the dynamic power dissipation is the circuits based on adiabatic logic. The logic circuits based on adiabatic logic are gaining prime importance due to their low power dissipation characteristic. Adiabatic logic reduces the energy dissipation by reducing the dissipation across resistances of conducting MOSFETs and recovering the part of energy given to the output back to the source, which extends the battery life. Several adiabatic logic styles have been reported by different authors in their research work \cite{16}[17].

II. RULES OF ADIABATIC LOGIC DESIGN

In adiabatic circuits instead of dissipating the power is reused. By externally controlling the length and shape of signal transitions energy spent to flip a bit can be reduced to very small values. Since diodes are thermodynamically irreversible they are not used in the design of Adiabatic Logic. MOSFETs should not be turned ON when there is a significant potential difference between source and drain. And should not be turnoff when there is a significant current flowing through the device.

Figure 2. Charge Recovery Logic
Although diodes are fundamentally non-adiabatic, fortunately, transistors, despite being non-ideal switches, remain acceptable for adiabatic operation, so long as two basic rules are followed: (1) never turn on a transistor when there is a significant (non-negligible) voltage difference between its source and drain terminals. (2) Never turn off a transistor when there is significant current flowing through its channel.

Recently, power consumption has been a fundamental constraint in both high-performance and portable, energy-limited systems. In conventional CMOS circuits, power dissipation primarily occurs during device switching. A sudden flow of current through channel resistive elements results in half of the supplied energy being dissipated at each transition. In CMOS technology, as for energy dissipation, circuit designers are focusing on how to reduce VDD and CL. However, power dissipation can also be reduced by reducing the current flow into the transistors. Low-power circuit systems achieved by implementing the concept of adiabatic switching and energy recovery have been widely applied, and various energy-recovery circuits with adiabatic circuitry for ultra-low. Power implementation has been presented. The essential idea of adiabatic charging is to design a circuit that allows all the nodes to be charged or discharged at a constant current. Power dissipation is minimized by decreasing the peak current flow through transistors. This flow is accomplished by using ramp-like power/clock signals. The system draws some of the energy that is stored in the capacitors during a given computation step and uses this energy in subsequent computations. However, for a single and two-phase clock circuits, diode-based families have several disadvantages such as output amplitude degradation and the energy dissipation across the nodes in the charging path. However, for a single and two-phase clock circuits, diode-based families have several disadvantages such as output amplitude degradation and the energy dissipation across the nodes in the charging path. Proposed adiabatic logics that are easily derived from CMOS has how improvement in power dissipation as compared to different adiabatic logics. Proposed fundamental logic significantly exhibit lower power dissipation. [18].

III. VLSI CIRCUIT DESIGN FOR LOW POWER

Choices between static versus dynamic topologies, conventional CMOS versus pass-transistor logic styles and synchronous versus asynchronous timing styles have to be made during the design of a circuit. In static CMOS circuits, the component of power due to short circuit current is about the 10% of the total power consumption. However, in dynamic circuits we don't come across this problem, since there is no any direct dc path from supply voltage to ground. Only in domino-logic circuits there is such a path, in order to reduce sharing, hence there is a small amount of short-circuit power dissipation.

Another factor that fuels the need for low power chips is the increased market demand for portable consumer electronics powered by batteries. The craving for smaller, lighter and more durable electronic products indirectly translates to low power requirements. Battery life is becoming a product differentiator in many portable systems. Being the heaviest and biggest component in many portable systems, batteries have not experienced the similar rapid density growth compared to the electronic circuits. The main source of power dissipation in these high performance battery- portable digital systems running on batteries such as note-book computers, cellular phones and personal digital assistants are gaining prominence. For these systems, low power consumption is a prime concern, because it directly affects the performance by having effects on battery longevity. In this situation, low power VLSI design has assumed great importance as an active and rapidly developing field. In this article we discuss circuit and logic design approaches to minimize Dynamic, Leakage and Short Circuit power dissipation. Power optimization in a processor can be achieved at various abstract levels. System/Algorithm/Architecture has a large potential for power saving even these techniques tend to saturate as we integrate more functionality on an IC. So optimization at Circuit and Technology level is also very important for miniaturization of ICs.

Total Power dissipated in a CMOS circuit is sum total of dynamic power, short circuit power and static or leakage power. Design for low-power implies the ability to reduce all three components of power consumption in CMOS circuits during the development of a low power electronic product. In the sections to follow we summarize the most widely used circuit techniques to reduce each of these components of power in a standard CMOS design.
This paper is divided into six sections. Section 1, deals the introduction part. Section 2, Rules of Adiabatic logic Design. In section 3, VLSI circuit design for low power. In section 4, Proposed EEAL Based Master-Slave JK Flip Flop. In section 5, Proposed EEAL Based 3-bit Counter Conclusion is given in the section 6.

IV. PROPOSED EEAL BASED MASTER-SLAVE JK FLIP FLOP

The latches are generally designed by connecting two inverters or two NAND/NOR gates in a cross coupled manner. The proposed EEAL master slave JK flip flop was designed using proposed NAND gates and proposed inverter as shown in figure 4(a). The structure of proposed NAND gate is shown in figure 4(b). The inputs are J and K along with the clock signal clk. Q and Q' are the outputs where Q' is the complement of Q. The supply voltages are slowly varying complementary split level sinusoidal waveforms (V_P & V_P').

![Figure 4 (a)](image)

![Figure 4 (b)](image)

In order to realize operation of JK flip flop, consider the truth table for JK flip flop. It is required output follow the previous state when both input are ‘0’ and output become complement of previous state when both input are ‘1’. Simulated timing waveforms are shown in figure 4(b). The combination of inputs at each negative edge of clock pulse “J, 01, 11” are given in the form of strings. The output Q and Q' changes according to the inputs at each negative edge of clock pulse. Q= ‘1’ and Q’ = ‘0’ when J= ‘1’ and K = ‘0’. Similarly Q= ‘0’ and Q’ = ‘1’ when J= ‘0’ and K = ‘1’. Output Q will be complemented when J= ‘1’ and K = ‘1’. Further the outputs Q and Q’ are lathed to their corresponding values other than the negative edges of clock pulses.

V. PROPOSED EEAL BASED 3-BIT COUNTER

The proposed 3 bit binary up counter can be designed by using 3 proposed JK flip flop for each binary bit shown in figure 5(a). This counter will increment once for every clock cycle and count from zero to seven before it overflows. A power supply clock is as split level sinusoidal waveforms (V_P & (V_P')).

![Figure 4 (c)](image)

![Table 4 (d)](image)

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Power consumed (µW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS JK flip flop</td>
<td>10.22</td>
</tr>
<tr>
<td>Proposed JK flip flop</td>
<td>4.39</td>
</tr>
</tbody>
</table>

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Simulation results obtained from the proposed sequential circuits have got strong validation and give low power dissipation at low frequencies range. The comparison of the proposed circuit with other traditional methodologies has proved that power consumption with the proposed logic is far less as compared to other CMOS circuit. In conclusion, an energy efficient adiabatic technique that would reduce the power consumption. It was found that the proposed adiabatic logic style is advantageous when applied to low-power digital devices operated at low frequencies. In future these logics can be designed at other technologies to further reduce the power consumption and voltage swing can be improved and further work on minimization of chip area can also be done on various technologies.

REFERENCES


