Stability of A Differential Eight Transistor Sram Cell

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Abstract—Static Random Access Memories are available in every portable as well as digital equipments. Their efficiency affects the overall system efficiency. In VLSI, the performance metrics are in terms of function, speed, area and power. The function of a differential eight transistor SRAM cell is analysed in this paper by measuring it’s stability in sub threshold operation. The SNM of the cell is measured by graphical method and it is compared with the SNM of the conventional six transistor cell. There is small delay overhead due to the isolating transistor added. The simulation tool used is Tanner V13.0and the waveforms are produced.

Keywords—Static Random Access Memories, Differential Eight Transistor cell, Sub threshold, SNM, delay overhead, isolation Transistor

I. INTRODUCTION

In the era of anywhere, anytime computing, the demand for electronic and multimedia devices is exponentially growing. These devices have to be portable as well as perform multiple functions. These facts have made the CMOS IC technology scale down aggressively entering into the nano meter regime during this decade[1]. Higher performance and more features are expected by the consumers. Density and speed of IC’s have been increasing exponentially for over three decades. This observation is made by the Moore’s law.

For this device scaling, the two parameters that are treated are the size of the transistor and the operating voltage. The dimension reductions directly has a impact on the data stability. Current system on chip trend result in a significant percentage of the total die area being dedicated to memory blocks[1]. Today, no digital system is built without memory.

Static Random Access Memories are the predominant technologies used to implement memory cells. SRAM caches influence the system speed and power consumption in modern computer system.

The SRAM parameter variations dominate the overall circuit parameter characteristics as more and more area is dedicated to memory in the forthcoming generations. Therefore, a deep knowledge and analysis about the stability of the SRAM cells is a must[1]

The paper is organized as follows, the second section introduces the sub threshold operation, section III discusses the proposed structure, section IV about the read operation and section V and VI deals with stability and the noise margins. The simulation and results are discussed in the section VII and VII.

II. SUB THRESHOLD OPERATION

Due to their growing embedded applications coupled with technology scaling challenges, considerable attention is given to the design of low power and high performance SRAMs. The shrinking of the devices is limited by the amount of power dissipation. So, scaling is achieved by operating the device in the Sub threshold region. Here, the supply voltage Vdd of the circuit in question is set at a value lower than or equal to the threshold voltage of that particular process technology.(ie)Vdd less than Vθ.

The Circuit will operate with only Sub threshold leakage currents. This approach not only results in very low power consumption but it also utilizes leakage currents for computation and thus capitalizes on the problem that traditional VLSI design methodologies are faced with.

The amount of Sub threshold conduction is set by the threshold voltage, which sits between ground and the supply voltage and so has to be reduced along with the supply voltage. That reduction means less gate voltage swing below threshold to turn the device off, and as sub threshold conduction varies exponentially with gate voltage swing below threshold to turn the devices off and as sub threshold conduction varies exponentially with gate voltage it becomes more and more significantly as mosfets shrinks in size.

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III. PROPOSED CELL TOPOLOGY

The proposed D8T cell breaks the feedback loop of the cell during the read operation to guarantee the stability of the stored data.

IV. READ OPERATION

Simulation waveforms of the cell node voltages and bit lines during a read operation with a supply voltage of VDD = 0.3 V and a noise source of Vn = 150mv at the internal nodes of the cell. Upon activation of the WL and deactivation of the RWL, M8 separates Q from Q2 and the charge at Q2 is secured near VDD during the read operation.

The sensing problem in the traditional eight transistor cell with separate read port is overcome in the proposed topology. The simulation for reading logic ‘0’ and logic ‘1’ is shown in the waveforms.

V. STABILITY

The scaling of CMOS technology has enabled the improvement in the speed and device density in the integrated circuits. The downside of this scaling is the increase in the Subthreshold leakage of the transistor due to the constant reduction in the channel length. The improvement in the energy efficiency in the Subthreshold processors, come at a cost of considerable increase in delay. There is also the issue of increased sensitivity of the circuit to variations. The noise margin stability of the bit cell decreases as we scale down to low voltages. The voltage noise margin for the SRAMs has the upper limit of 0.5 * Vdd.

As we scale down our supply voltages, the noise margin decreases to modest values. Due to this reduced noise margin, the probability of read/write failure in the presence of threshold voltage variations increases.

The Stability of Hold/Standby mode can be measured by Static Noise Margin (SNM). The Read and Write Stability can be measured by Read and Write margin. If a noise is present long enough to read, such type of noise is called Static or Dc noise. The offsets and mismatches due to processing and variations in an SRAM’s operating conditions are the Static Noise present in the Cell.

VI. NOISE MARGIN

A. Static Noise Margin : It is defined as the minimum DC noise voltage necessary to flip the state of the cell. The Static Noise Margin is determined by Graphical method.

The SRAM Cell consists of two inverter connected to form a Bi stable Latch. The SNM of the cell is defined as the maximum value of the noise voltage that can be tolerated by the latch before changing state. If the input impedance of the inverters is much larger than their output impedance, a graphical method can be applied to determine the SNM of the latch. The Voltage Transfer Curve should include the normal and mirrored inverter characteristics.

VII. SIMULATION RESULT

The following figures show the transient response of 6T and D8T SRAM cell to read a logic ‘0’. Table 1 gives the comparison of Delay, Average Power and SNM of conventional six transistor cell and the proposed eight transistor topology.
From the waveforms it can be observed that the proposed topology introduces a small delay due to the extra NMOS transistors added. The average power is reduced in the D8T cell, but the stability is improved. The read margin of the Differential Eight Transistor is more than the conventional Six Transistor cell under the same voltage and temperature conditions. The simulation is done using PTM 45 m metal gate model card.

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